Single Buck Voltage Mode PWM Controller TD1720

General Description

The TD1720 is a voltage mode, fixed 300kHz switching frequency, synchronous buck converter. The TD1720 allows wide input voltage that is either a single 5~12V or two supply voltage(s) for various applications. A power-on-reset (POR) circuit monitors the VCC supply voltage to prevent wrong logic controls. A builtin soft-start circuit prevents the output voltages from overshoot as well as limits the input current. An internal 0.8V temperature-compensated reference voltage with high accuracy is designed to meet the requirement of low output voltage applications. The TD1720 provides excellent output voltage regulations against load current
variation.

The controller's over-current protection monitors the output current by using the voltage drop across the RDS(ON) of low-side MOSFET, eliminating the need for a current sensing resistor that features high efficiency and low cost. In addition, the TD1720 also integrates excellent protection functions: The over-voltage protection (OVP) , under- voltage protection (UVP). OVP circuit which monitors the FB voltage to prevent the PWM output from overvoltage,and UVP circuit which monitors the FB voltage to prevent the PWM output from under-voltage or short-circuit.The TD1720 is available in SOP-8P and TDFN3x3-10 packages.

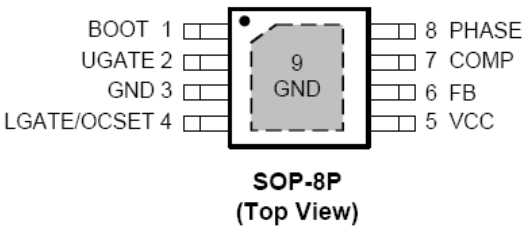
Features

- Wide 5V to 12V Supply Voltage
- Power-On-Reset Monitoring on VCC
- Excellent Output Voltage Regulations 0.8V Internal Reference ±1% Over-Temperature Range
- Integrated Soft-Start
- Voltage Mode PWM Operation with External Compensation
- Up to 90% Duty Ratio for Fast Transient Response
- Constant Switching Frequency 300kHz ±10%
- Drive Dual Low Cost N-MOSFETs with Adaptive Dead-Time Control
- 50% Under-Voltage Protection
- 125% Over-Voltage Protection
- Adjustable Over-Current Protection Threshold Using the RDS(ON) of Low-Side MOSFET
- Shutdown Control by COMP
- Power Good Monitoring (TDFN-10 3mmx3mm Package Only)
- SOP-8P and TDFN3x3-10 Packages
- Lead Free and Green Devices Available (RoHS Compliant)

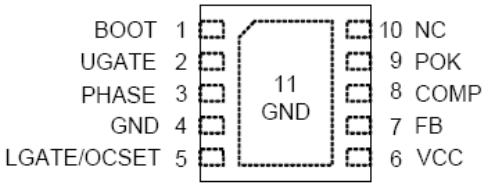
Applications

- Graphic Cards
- DSL, Switch HUB
- Wireless Lan
- Notebook Computer
- Mother Board
- LCD Monitor/TV

Pin Assignments



SOP-8P
(Top View)



TDFN3x3-10
(Top View)

PIN NO.		NAME	FUNCTION
SOP-8P	TDFN3x3-10		
1	1	BOOT	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal diode, generates the bootstrap voltage for the high-side
2	2	UGATE	High-side Gate Driver Output. This pin is the gate driver for high-side
3	4	GND	Signal and Power ground. Connecting this pin to system ground.
4	5	LGATE	Low-side Gate Driver Output and Over-Current Setting Input. This pin is the gate driver for low-side MOSFET. It also used to set the maximum inductor current. Refer to the section in "Function Description" for detail.
5	6	VCC	Power Supply Input. Connect a nominal 5V to 12V power supply voltage to this pin. A power-on-reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10 F) is connected to GND for noise decoupling.
6	7	FB	Feedback Input of Converter. The converter senses feedback voltage via FB and regulates the FB voltage at 0.8V. Connecting FB with a resistor-divider from the output sets the output voltage of the converter.
7	8	COMP	This is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin. Pulling COMP low ($V_{DISABLE}$ = 0.4V max.) will shut down the controller. When the pull-down device is released, the COMP pin will start to rise. When the COMP pin rises above the $V_{DISABLE}$ trip point, the TD1720 will begin a new initialization and soft-start cycle.

8	3	PHASE	This pin is the return path for the high-side gate driver. Connecting this pin to the high-side MOSFET source and connect a capacitor to BOOT for the bootstrap voltage. This pin is also used to monitor the voltage drop across the low-side MOSFET for over-current protection.
9(Exposed Pad)	11(Exposed Pad)	GND	Thermal Pad. Connect this pad to the system ground plan for good thermal conductivity.
-	9	POK	POK is an open drain output used to indicate the status of the output voltage. Connect the POK pin to 5 to 12V through a pull-high resistor.
-	10	NC	No Connect

Ordering Information

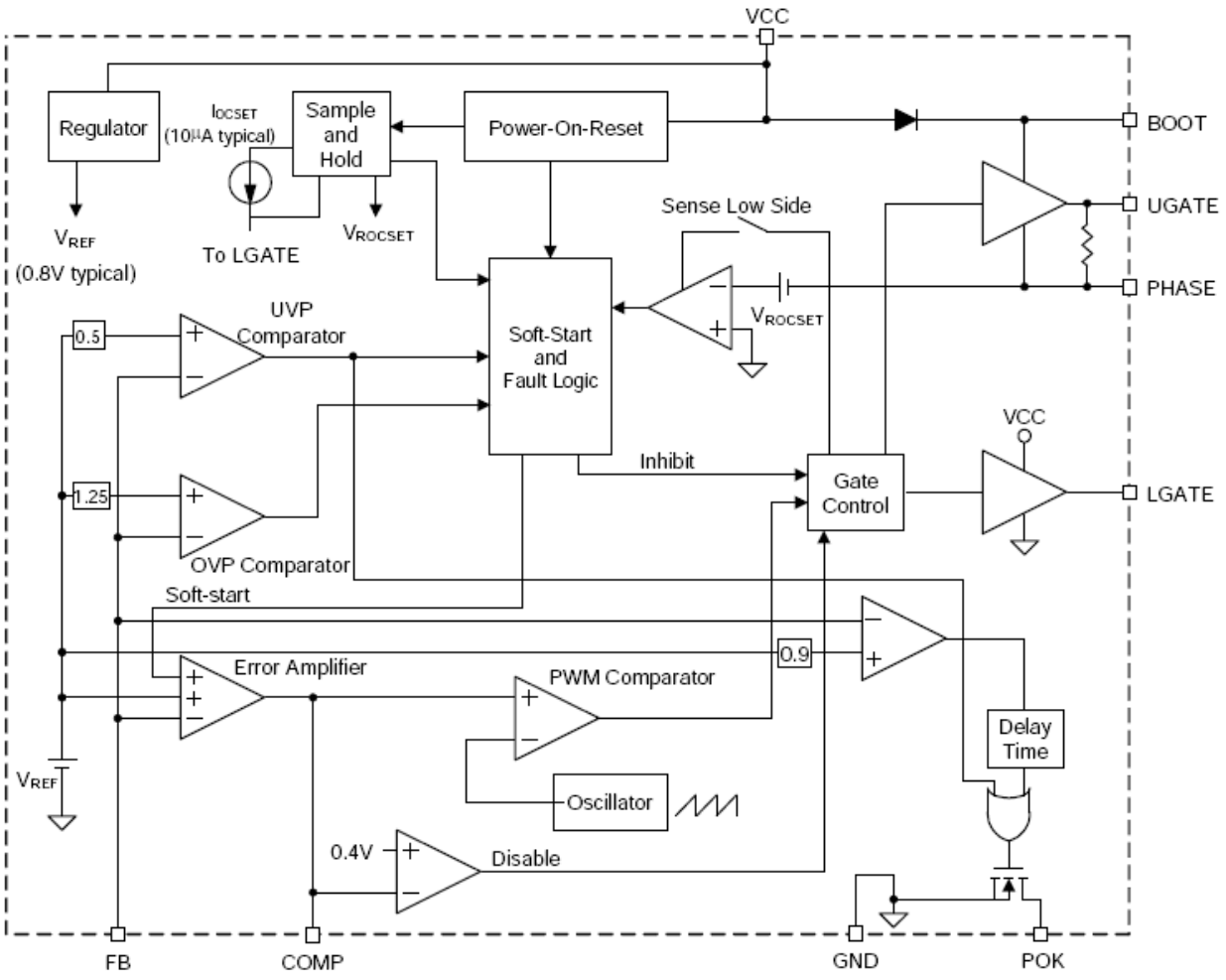
TD1720 □ □

Circuit Type

Package
M:SOP8-PP
Q:TDFN

Packing:
Blank：Tube
R:Type and Reel

Functional Block Diagram



Functional Block Diagram of TD1720

Absolute Maximum Ratings

Symbol	Parameter		Rating	Unit
V_{VCC}	VCC Supply Voltage (VCC to GND)		-0.3 ~ 16	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)		-0.3 ~ 16	V
	BOOT Supply Voltage (BOOT to GND)		-0.3 ~ 30	V
V_{UGATE}	UGATE Voltage (UGATE to PHASE)	> 20ns	-0.3 ~ V_{BOOT}+0.3	V
		< 20ns	-5 ~ V_{BOOT}+5	V
V_{LGATE}	LGATE Voltage (LGATE to GND)	> 20ns	-0.3 ~ V_{VCC}+0.3	V
		< 20ns	-5 ~ V_{VCC}+5	V
V_{PHASE}	PHASE Voltage (PHASE to GND)	> 20ns	-0.3 ~ 16	V
		< 20ns	-5 ~ 21	V
	FB and COMP to GND		-0.3 ~ 7	V
	POK to GND		-0.3~V_{CC}+0.3	V
T_J	Maximum Junction Temperature		150	℃
T_{STG}	Storage Temperature		-65 ~ 150	℃
T_{SDR}	Maximum Lead Soldering Temperature, 10 Seconds		260	℃

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recom- mended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
VIN	VIN Supply Voltage	3.3 ~ 13.2	V
VVCC	VCC Supply Voltage	4.5 ~ 13.2	V
VOUT	Converter Output Voltage	0.8 ~ 5.5	V
IOUT	Converter Output Current	0 ~ 20	A
TA	Ambient Temperature	-40 ~ 85	℃
TJ	Junction Temperature	-40 ~ 125	℃

Note : Refer to the application circuit for further information.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance -Junction to Ambient (Note 2) SOP-8P	60	°C/W

Note :$\theta_{JA}$is measured with the component mounted on a high effective thermal conductivity test board in free air.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	TD1720			Unit
			Min.	Typ.	Max.	
INPUT SUPPLY VOLTAGE AND CURRENT						
I_{VCC}	VCC Supply Current (Shutdown Mode)	UGATE and LGATE open; COMP=GND	-	-	700	uA
	VCC Supply Current	UGATE and LGATE open	-	2	3	mA
POWER-ON-RESET(POR)						
	Rising VCC POR Threshold		3.8	4.1	4.4	V
	VCC POR Hysteresis		0.3	0.5	0.6	V
OSCILLATOR						
F_{OSC}	Oscillator Frequency		270	300	330	kHz
V_{OSC}	(Note 4)	(1.2V~2.7V typical)	-	1.5	-	V
D_{MAX}	Maximum Duty Cycle		-	-	90	%
REFERENCE						
V_{REF}	Reference Voltage	T_A = -40 ~ 85°C	0.792	0.8	0.808	V
	Converter Line/Load Regulation	V_{CC}=4.5~13.2V, I_{OUT} = 0 ~	-0.2	-	0.2	%
ERROR AMPLIFIER						
gm	Transconductance (Note)		-	667	-	A/V
	Open-Loop Bandwidth (Note)	R_L = 10k , C_L = 10pF	-	20	-	MHz
	FB Input Leakage Current	V_{FB} = 0.8V	-	-	0.1	uA
	COMP High Voltage	R_L = OPEN	-	3	-	V
	COMP Low Voltage	R_L = OPEN	-	1.5	-	
	Maximum COMP Source Current	V_{COMP} = 2V	-	200	-	uA
	Maximum COMP Sink Current	V_{COMP} = 2V	-	200	-	

Electrical Characteristics(Cont.)

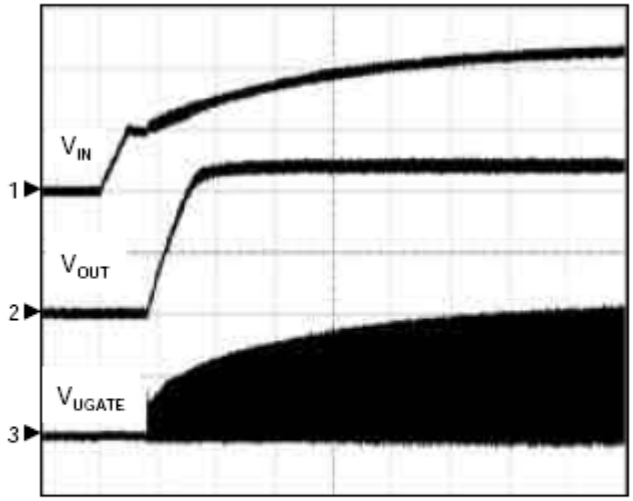
Refer to the typical application circuit. These specifications apply over V_{VCC} = 12V, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	TD1720			Unit
			Min.	Typ.	Max.	
GATE DRIVERS						
	High-Side Gate Driver Source	$V_{BOOT-GND}$= 12V, $V_{UGATE-PHASE}$ = 6V	-	1.0	-	A
	High-Side Gate Driver Sink Current	$V_{BOOT-GND}$= 12V $V_{UGATE-PHASE}$ = 6V	-	1.1	-	
	Low-Side Gate Driver Source	V_{VCC} = 12V, $V_{LGATE-GND}$ = 6V	-	1.5	-	A
	Low-Side Gate Driver Sink Current	V_{VCC} = 12V, $V_{LGATE-GND}$ = 6V	-	1.8	-	
T_D	Dead-Time (Note 4)		-	30	-	ns
PROTECTIONS						
V_{FB_UV}	FB Under-Voltage Protection Trip	Percentage of V_{REF}	40	45	50	%
	Under-Voltage Debounce Interval		-	2	-	s
	Under-Voltage Protection Enable Delay	The same as soft -start interval	1	1.5	2	ms
V_{FB_OV}	FB Over-Voltage Protection Trip	V_{FB} rising	115	125	135	%
	FB Over-Voltage Protection		-	5	-	%
	Over-Voltage Debounce Interval		-	2	-	s
V_{OCP_MAX}	Built-in Maximum OCP Voltage		350	-	-	mV
I_{OCSET}	OCSET Current Source		9	10	11	uA
SOFT-START						
$V_{DISABLE}$	Shutdown Threshold of V_{COMP}		-	-	0.4	V
T_{SS}	Internal Soft-Start Interval (Note 4)		1	1.5	2	ms
POWER OK INDICATOR (POK) (ONLY FOR TDFN3X3-10 PACKAGE)						
I_{POK}	POK Leakage Current	V_{POK}=5V	-	0.1	1	uA
V_{POK}	POK Threshold	VFB is from low to target value (POK Goes High)	85	90	95	%
		VFB Falling, POK Goes Low	45	50	55	%
		VFB Rising, POK Goes Low	120	125	130	%
	POK Delay Time		1	3	5	ms

Note 4: Guaranteed by design, not production tested.

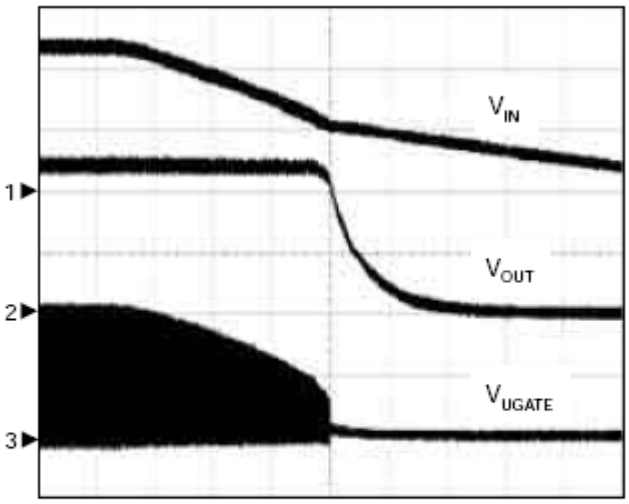
Typical Operating Characteristics

Power On



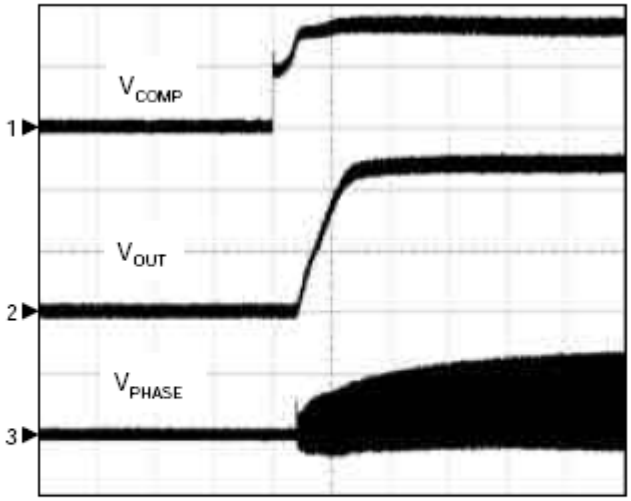
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{UGATE}, 10V/Div
TIME: 1ms/Div

Power Off



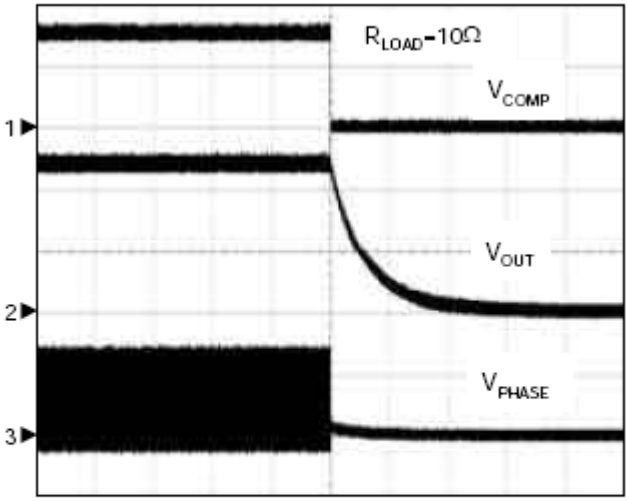
CH1: V_{IN}, 5V/Div
CH2: V_{OUT}, 500mV/Div
CH3: VU_{GATE}, 10V/Div
TIME: 2ms/Div

Enable



CH1: V_{COMP}, 1V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{PHASE}, 10V/Div
TIME: 1ms/Div

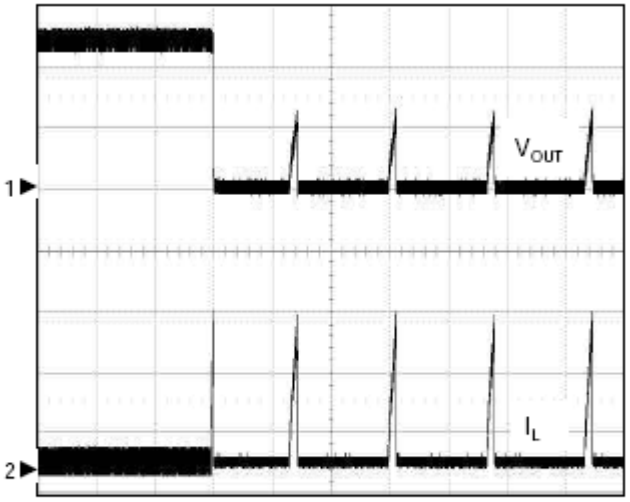
Shutdown



CH1: V_{COMP}, 1V/Div
CH2: V_{OUT}, 500mV/Div
CH3: V_{PHASE}, 10V/Div
TIME: 2ms/Div

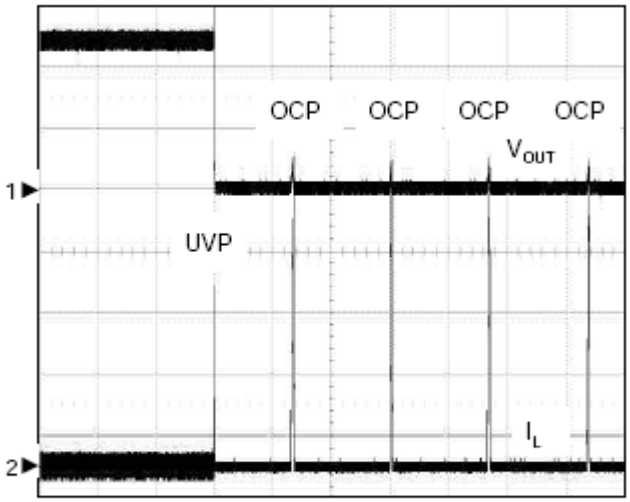
Typical Operating Characteristics(Cont.)

Over-Current Protection



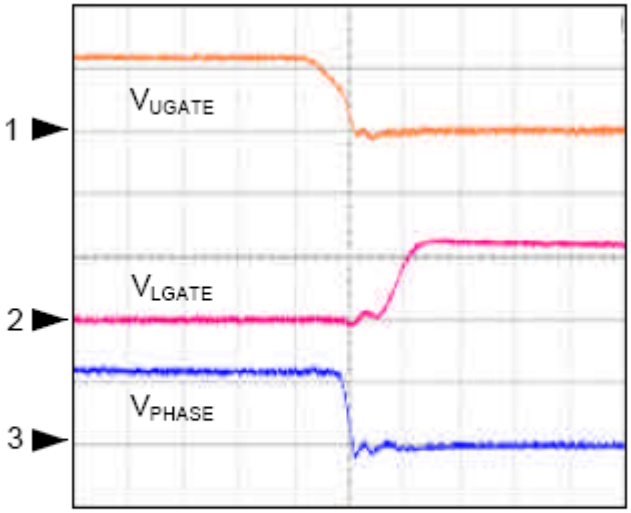
CH1: V_{OUT}, 500mV/Div
CH2: I_L, 10A/Div
TIME: 5ms/Div

Under-Voltage Protection



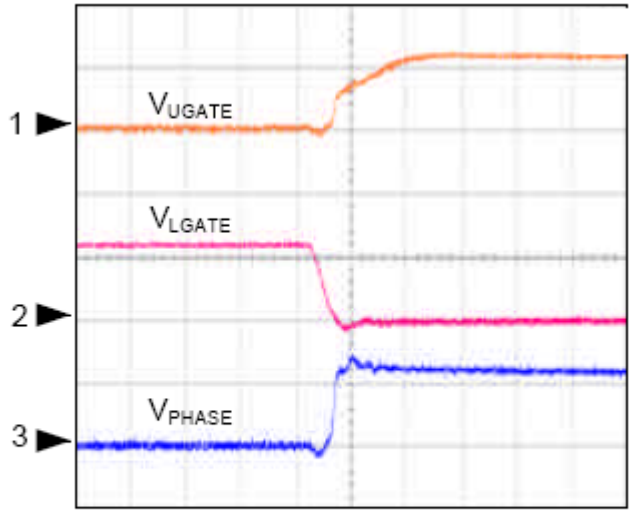
CH1: V_{OUT}, 500mV/Div
CH2: I_L, 10A/Div
TIME: 5ms/Div

UGATE Falling



CH1: V_{UGATE}, 20V/Div
CH2: V_{LGATE}, 10V/Div
CH3: V_{PHASE}, 10V/Div
TIME: 50ns/Div

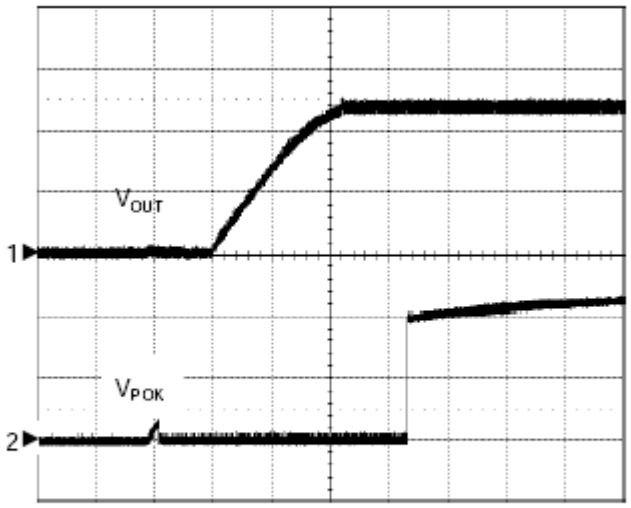
UGATE Rising



CH1: V_{UGATE}, 20V/Div
CH2: V_{LGATE}, 10V/Div
CH3: V_{PHASE}, 10V/Div
TIME: 50ns/Div

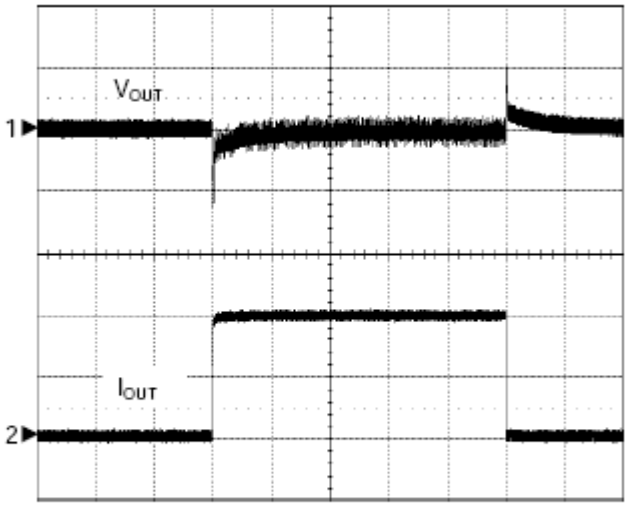
Typical Operating Characteristics(Cont.)

Power OK



CH1: V_{OUT}, 500mV/Div
CH2: V_{POK}, 5V/Div
TIME: 1ms/Div

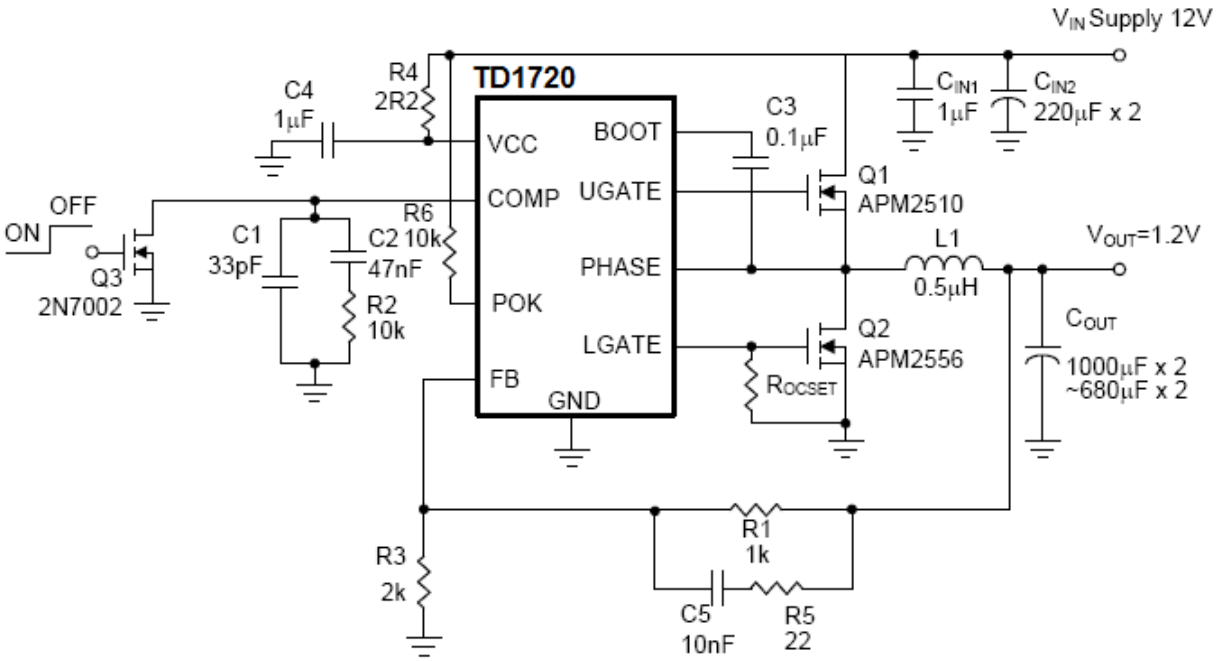
Load Transient



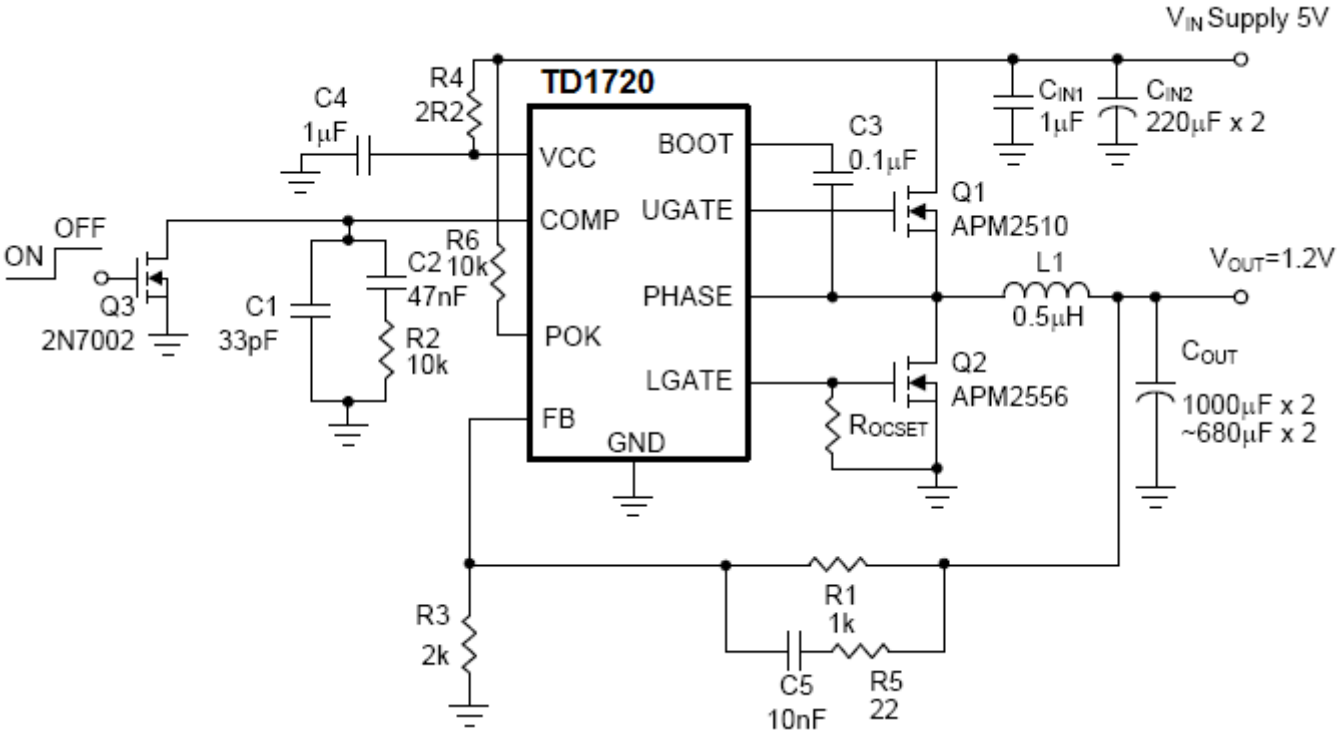
CH1: V_{OUT}, 50mV/Div, AC
CH2: I_{OUT}, 5A/Div
TIME: 200μs/Div

Typical Application Circuit

TD1720 12V Application Circuit



TD1720 5V Application Circuit



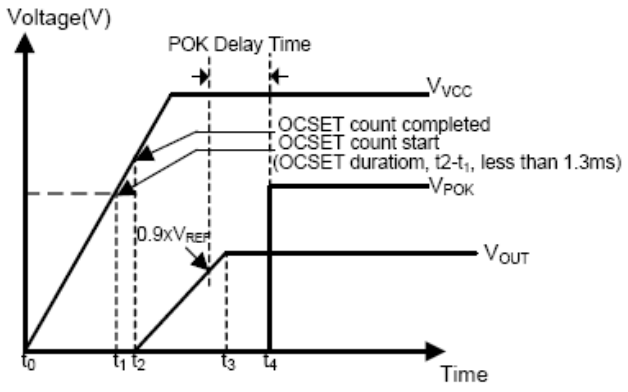
Function Description

Power-On-Reset (POR)

The Power-On-Reset (POR) function of TD1720 continually monitors the input supply voltage (VCC) and ensures that the IC has sufficient supply voltage and can work well. The POR function initiates a soft-start process while the VCC voltage just exceeds the POR threshold; the POR function also inhibits the operations of the IC while the VCC voltage falls below the POR threshold.

Soft-Start

The TD1720 builds in a soft-start function about 1.5ms (Typ.) interval, which controls the output voltage rising as well as limiting the current surge at the start-up. During soft-start, an internal ramp voltage connected to the one of the positive inputs of the error amplifier replaces the reference voltage (0.8V typical) until the ramp voltage reaches the reference voltage. The soft-start circuit interval is shown as figure 1. The UVP function enable delay is from t2 to t3.



Over-Current Protection of the PWM Converter

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drainto-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET during it's on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor required.

A resistor (R_{OCSET}), connected from the LGATE/OCSET to GND, programs the over-current trip level. Before the IC initiates a soft-start process, an internal current source, I_{OCSET} (10μA typical), flowing through the R_{OCSET} develops a voltage (V_{ROCSET}) across the R_{OCSET}. The device holds V_{ROCSET} and stops the current source I_{OCSET} during normal operation. When the voltage across the low-side MOSFET exceeds the V_{ROCSET}, the TD1720 turns off the highside and low-side MOSFET,and the device will enters hiccup mode until the over-current phenomenon is released.

The TD1720 has an internal OCP voltage, V_{OCP_MAX}, and the value is 0.35V (minimum). When the R_{OCSET} x I_{OCSET} exceed 0.35V or the R_{OCSET} is floating or not connected, the V_{ROCSET} will be the default value 0.35V. The over current threshold would be 0.35V across low-side MOSFET. The threshold of the valley inductor current-limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(low-side)}$$

For the over-current is never occurred in the normal operating load range, the variation of all parameters in the above equation should be considered:

- The $R_{DS(ON)}$ of low-side MOSFET is varied by temperature and gate to source voltage. Users should determine the maximum $R_{DS(ON)}$ by using the manufacturer's datasheet.
- The minimum I_{OCSET} (9μA) and minimum R_{OCSET} should be used in the above equation.
- Note that the I_{LIMIT} is the current flow through the lowside MOSFET; I_{LIMIT} must be greater than valley inductor current which is output current minus the half of inductor ripple current.

$$I_{LIMIT} > I_{OUT(MAX)} - \frac{\Delta I}{2}$$

Where ΔI = output inductor ripple current

- The overshoot and transient peak current also should be considered.

Function Description(Cont.)

Under-Voltage Protection

The under-voltage function monitors the voltage on FB (V_{FB}) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the V_{FB} falls below the falling UVP threshold (50% V_{REF}), a fault signal is internally generated and the device turns off highside and low-side MOSFETs. The device will enters hiccup mode until the under-voltage phenomenon is released.

Over-Voltage Protection (OVP) of the PWM Converter

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage condition. When the output voltage rises above 125% of the nominal output voltage, the TD1720 turns off the high-side MOSFET and turns on the low-side MOSFET until the output voltage falls below the falling OVP threshold.

Shutdown and Enable

The TD1720 can be shut down or enabled by pulling low the voltage on COMP. The COMP is a dual-function pin. During normal operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin. Pulling the COMP low ($V_{DISABLE}$ = 0.4V maximum) places the controller into shutdown mode which UGATE and LGATE are pulled to PHASE and GND respectively. When the pull-down device is released, the COMP voltage will start to rise. When the COMP voltage rises above the $V_{DISABLE}$ threshold, the TD1720 will begin a new initialization and soft-start process.

Adaptive Shoot-Through Protection of the PWM Converter

The gate drivers incorporate an adaptive shoot-through protection to prevent high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off the low-side MOSFET, the LGATE voltage is monitored until it is below 1.5V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off of the high-side MOSFET, the UGATE-to-PHASE voltage is also monitored until it is below 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

Power OK Indicator

The TD1720 features an open-drain POK output pin to indicate one of the IC's working statuses including soft-start, under-voltage fault, over-current fault. In normal operation, when the output voltage rises 90% of its target value, the POK goes high. When the output voltage outruns 50% or 125% of the target voltage, POK signal will be pulled low immediately.

Application Information

Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.8V. The output voltage is determined by:

$$V_{OUT} = 0.8 \times \left(1 + \frac{R_1}{R_2}\right)$$

Where R1 is the resistor connected from V_{OUT} to FB and R2 is the resistor connected from FB to the GND.

Output Capacitor Selection

The selection of C_{OUT} is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications.multiple capacitors have to be paralleled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt,consult the capacitors manufacturer.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation,select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately $I_{OUT}/2$ where I_{OUT} is the load current. During power up, the input capacitors have to handle large amount of surge current.If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.For high frequency decoupling, a ceramic capacitor between 0.1μF to 1μF can connect between VCC and ground pin.

Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

where Fs is the switching frequency of the regulator.

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

A tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network between COMP pin and ground should be added. The simplest loop compensation network is shown in Figure 5.The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer function are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The FLC is the double poles of the LC filter, and FESR is the zero introduced by the ESR of the output capacitor.

Application Information(Cont.)

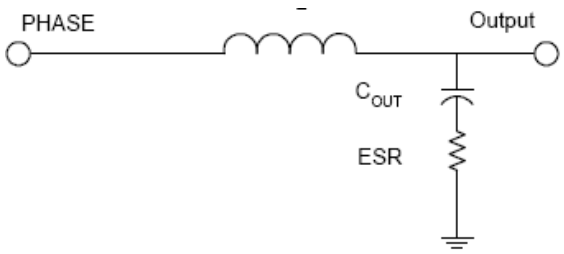


Figure 2. The Output LC Filter

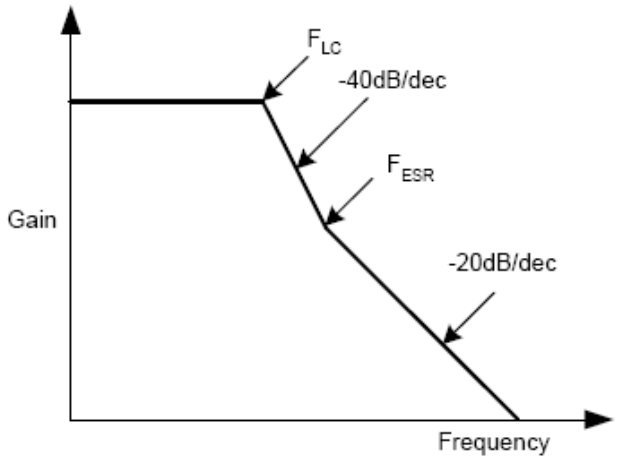


Figure 3. The LC Filter Gain & Frequency

The PWM modulator is shown in Figure 4. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

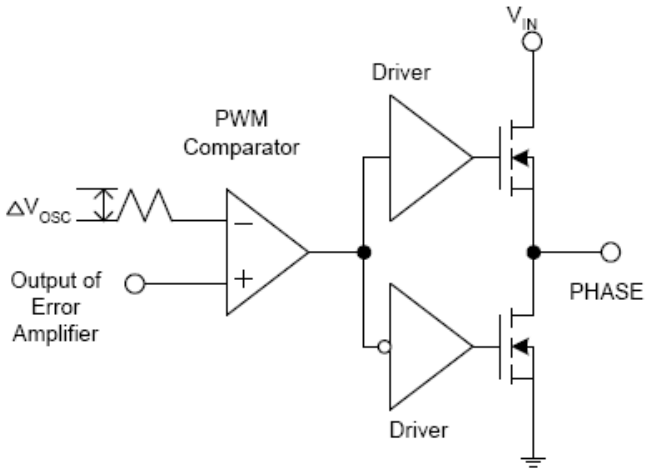


Figure 4. The PWM Modulator

The compensation circuit is shown in Figure 5. R2 and C2 introduce a zero and C1 introduces a pole to reduce the switching noise. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = gm \times Z_O = gm \times \left[\left(R2 + \frac{1}{sC2}\right) // \frac{1}{sC1}\right]$$

$$= gm \times \frac{\left(s + \frac{1}{R2 \times C2}\right)}{s \times \left(s + \frac{C2 + C1}{R2 \times C1 \times C2}\right) \times C1}$$

The pole and zero of the compensation network are:

$$F_P = \frac{1}{2 \times \pi \times R2 \times \frac{C1 \times C2}{C1 + C2}}$$

$$F_Z = \frac{1}{2 \times \pi \times R2 \times C2}$$

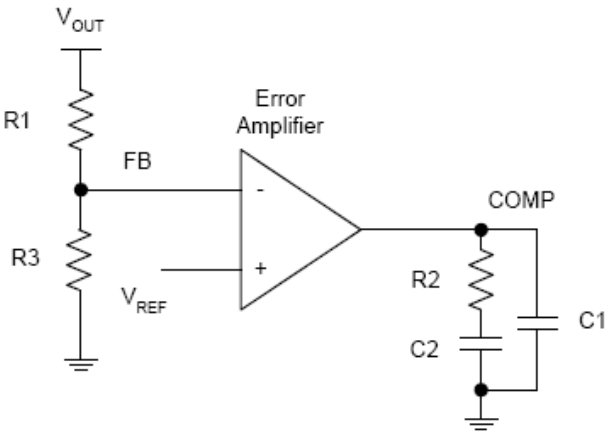


Figure 5. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times \frac{R3}{R1 + R3} \times GAIN_{AMP}$$

Figure 6 shows the converter gain and the following guidelines will help to design the compensation network.

1.Select the desired zero crossover frequency F_O:

(1/5 ~ 1/10) x F_{SW} >F_O>F_Z

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_{ESR}}{F_{LC}^2} \times \frac{R1 + R3}{R3} \times \frac{F_O}{gm}$$

Where:gm = 667μA/V

Application Information(Cont.)

2. Place the zero F_Z before the LC filter double poles F_{LC}:

$F_Z = 0.75 \times F_{LC}$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times 0.75 \times F_{LC}}$$

3. Set the pole at the half the switching frequency:

$F_P = 0.5 \times F_{SW}$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{\pi \times R2 \times C2 \times F_{SW} - 1}$$

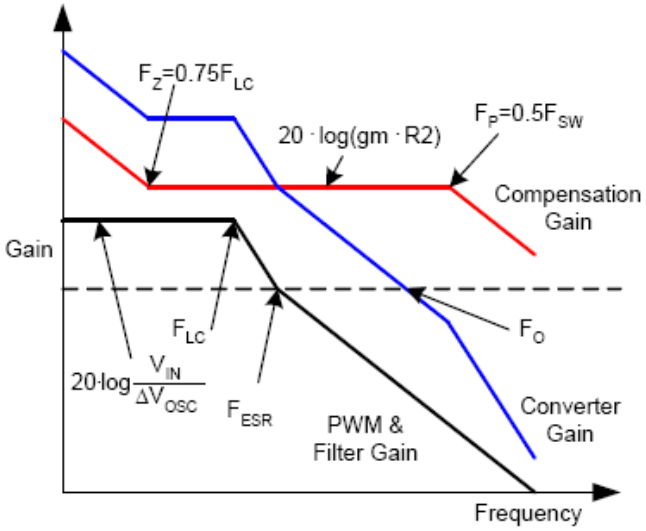


Figure 6. Converter Gain & Frequency

MOSFET Selection

The selection of the N-channel power MOSFETs is determined by the $R_{DS(ON)}$, reverse transfer capacitance (C_{RSS}), and maximum output current requirement.The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$P_{UPPER} = I_{OUT2}(1+ TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_{SW}$

$P_{LOWER} = I_{OUT2}(1+ TC)(R_{DS(ON)})(1-D)$

where I_{OUT} is the load current

TC is the temperature dependency of $R_{DS(ON)}$

F_{SW} is the switching frequency

t_{sw} is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET includes an additional transition loss. The switching internal, t_{sw}, is the function of the reverse transfer capacitance C_{RSS}. Figure 7 illustrates the switching waveform internal of the MOSFET.

The (1+TC) term factors in the temperature dependency of the $R_{DS(ON)}$ and can be extracted from the "$R_{DS(ON)}$ vs Temperature" curve of the power MOSFET.

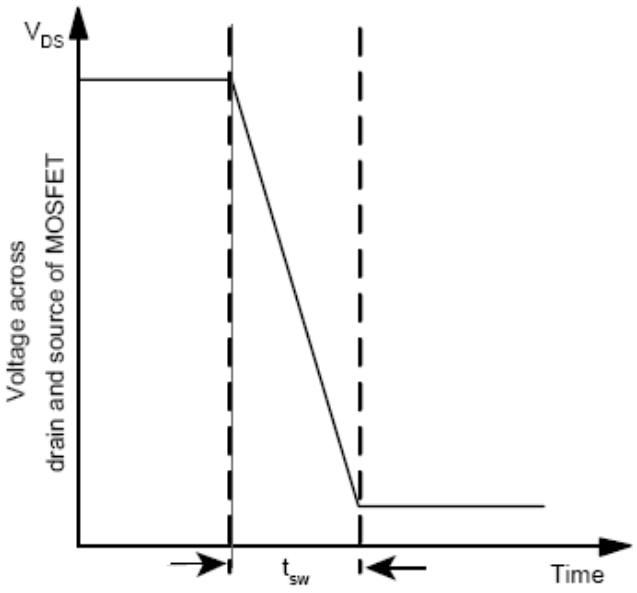


Figure 7. Switching Waveform Across MOSFET

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 300kHz,the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a

Application Information(Cont)

large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting imped ances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Figure 8. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UG and LG) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.

Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).

- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (V_{IN} and PHASE nodes) should be a large plane for heat sinking.
- The R_{OCSET} resistance should be placed near the IC as close as possible.

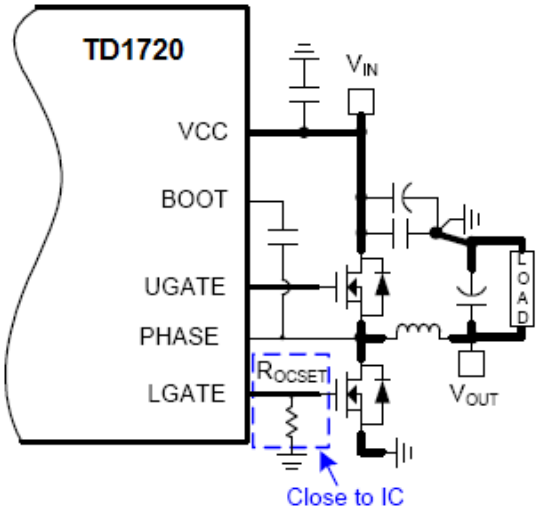
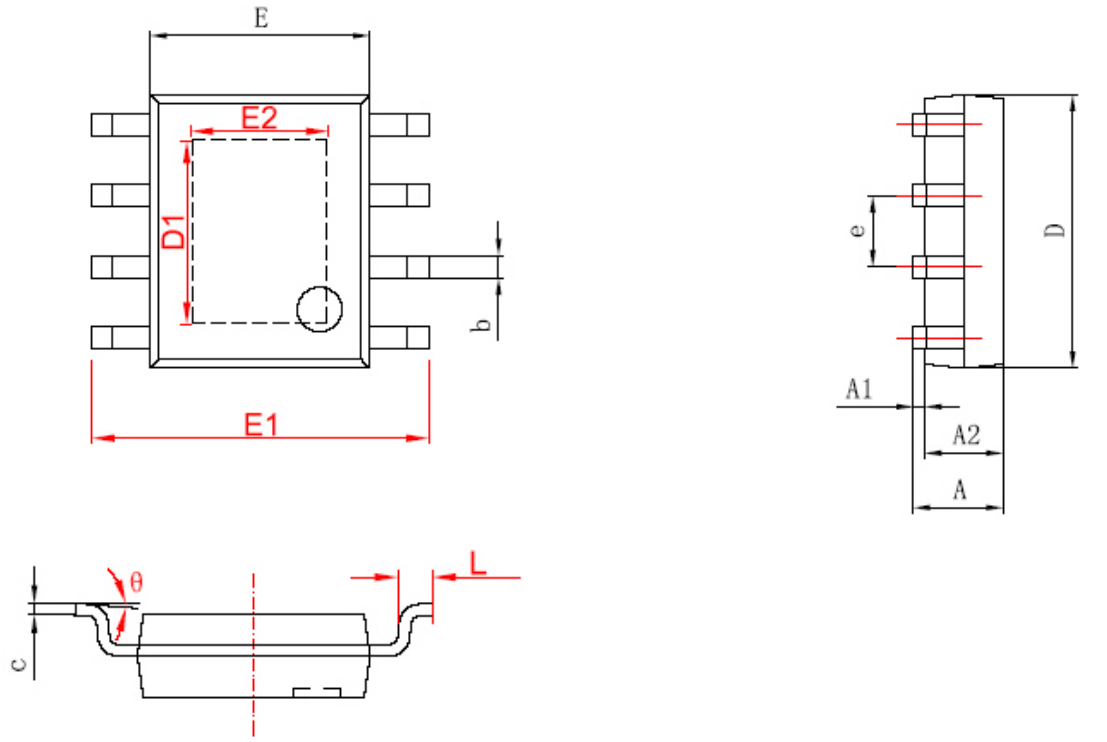


Figure 8. Layout Guidelines

Package Information

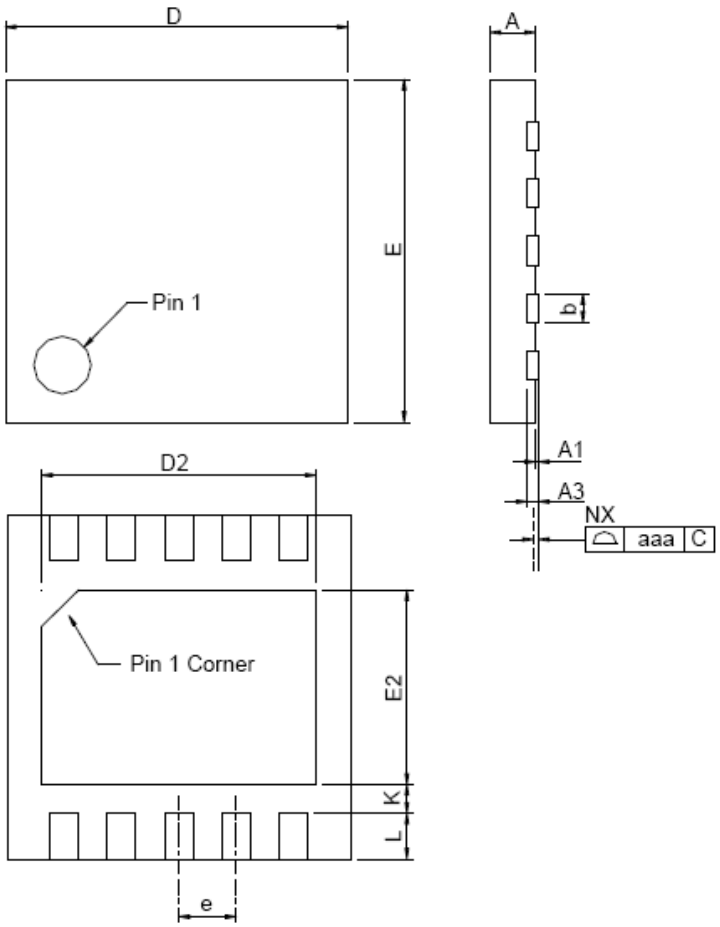
SOP8-PP Package Outline Dimensions



	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.050	0.150	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
D1	3.202	3.402	0.126	0.134
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.313	2.513	0.091	0.099
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Package Information

TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Design Notes

High-Performance PWM Controller TD1728

General Description

The TD1728 is a single-phase, constant-on-time, synchronous PWM controller, which drives N-channel MOSFETs. The TD1728 steps down high voltage to generate low-voltage chipset or RAM supplies in notebook computers.

The TD1728 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the TD1728 provides very high efficiency over light to heavy loads with loading- modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements.

The TD1728 is equipped with accurate positive current- limit, output under-voltage, and output over-voltage protections, perfect for NB applications. The Power-On-Reset function monitors the voltage on VCC to prevent wrong operation during power-on. The TD1728 has a 1ms digital soft-start and built-in an integrated output discharge method for soft-stop. An internal integrated soft-start ramps up the output voltage with programmable slew rate to reduce the start-up current. A soft-stop function actively discharges the output capacitors with controlled reverse inductor current.

The TD1728 is available in 10pin TDFN 3x3 package.

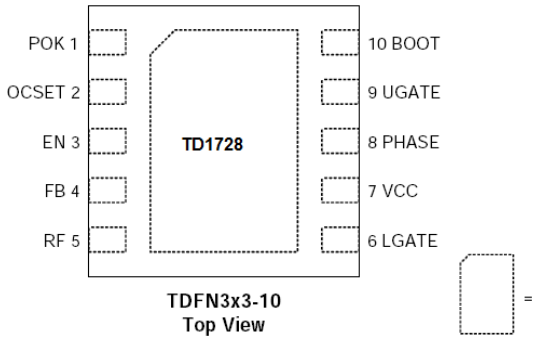
Features

- Adjustable Output Voltage from +0.7V to +5.5V
- 0.7V Reference Voltage
- ±1% Accuracy Over-Temperature
- Operates from an Input Battery Voltage Range of +1.8V to +32V
- Power-On-Reset Monitoring on VCC Pin
- Excellent Line and Load Transient Responses
- PFM Mode for Increased Light Load Efficiency
- Selectable PWM Frequency from 4 Preset Values
- Integrated MOSFET Drivers
- Integrated Bootstrap Forward P-CH MOSFET
- Adjustable Integrated Soft-Start and Soft-Stop
- Selectable Forced PWM or Automatic PFM/PWM Mode
- Power Good Monitoring
- 70% Under-Voltage Protection
- 125% Over-Voltage Protection
- Adjustable Current-Limit Protection
- Using Sense Low-Side MOSFET's $R_{DS(ON)}$
- Over-Temperature Protection
- TDFN-10 3x3 Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Notebook
- Table PC
- Hand-Held Portable
- AIO PC
- LCD Monitor / TV
- Battery Charger
- ADSL Modem
- Telecom / Networking Equipment

Pin Assignments



TDFN3x3-10
Top View

= GND and Thermal Pad (connected to GND plane for better heat dissipation)

PIN NO. TDFN3x3	PIN NO. TDFN2x2	NAME	FUNCTION
1	1	POK	Power Good Output. POK is an open drain output used to indicate the status of the output voltage. Connect the POK in to +5V through a pull-high resistor.
2	2	OCSET	Current-Limit Threshold Setting Pin. There is an internal source current 10 uA through a resistor from OCSET pin to GND. This pin is used to monitor the voltage drop across the Drain and Source of the low-side MOSFET for current-limit.
3	3	EN	Enable Pin of The PWM Controller. When the EN is above enable logic level, the Device is workable. When the EN is below shutdown logic level, the device is in shutdown and only low leakage current is taken from V_{CC} and V_{IN}.
4	4	FB	Output Voltage Feedback Pin. This pin is connected to the resistive divider that set the desired output voltage. The POK, UVP, and OVP circuits detect this signal to report output voltage status.
5	-	RF	This Pin is Allowed to Adjust The Switching Frequency. Connect a resistor R_{RF} to set switching frequency as show in Table1. The pin also controls forced PWM mode or PFM/PWM auto skip mode selection. When RF pin is pulled down to GND, the device is in automatic PFM/PWM Mode. When RF pin is pulled high to POK, the device is in force PWM mode.
6	6	LGATE	Output of The Low-side MOSFET Driver. Connect this pin to Gate of the low-side MOSFET. Swings from GND to VCC.
7	7	VCC	Supply Voltage Input Pin for Control Circuitry. Connect +5V from the VCC pin to the GND pin. Decoupling at least 1u F of a MLCC capacitor from the VCC pin to the GND pin.
8	8	PHASE	Junction Point of The High-side MOSFET Source, Output Filter Inductor and The Low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UGATE high-side gate driver.
9	9	UGATE	Output of The High-side MOSFET Driver. Connect this pin to Gate of the high-side MOSFET.
10	10	BOOT	Supply Input for The UGATE Gate Driver and An Internal Level-shift Circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
Exposed Pad	5	GND	Signal Ground for The IC

Ordering Information

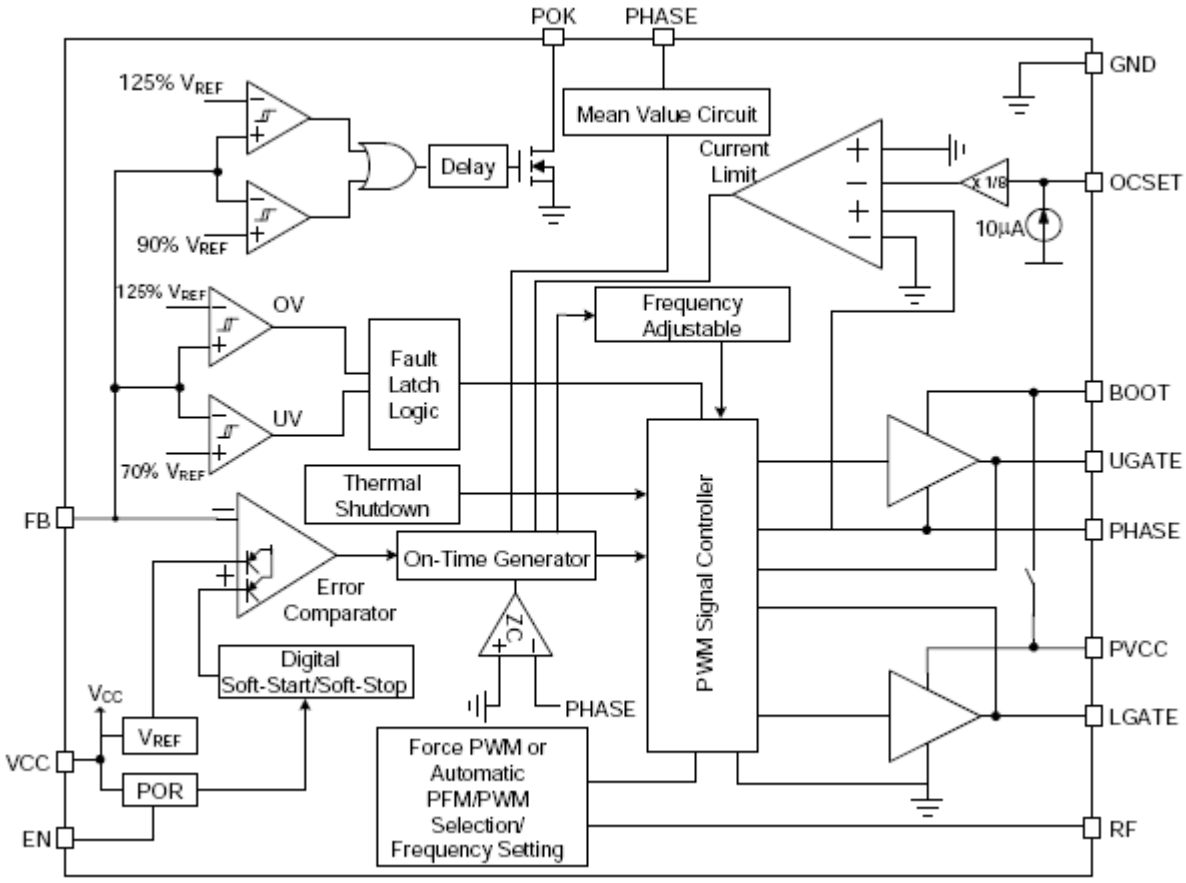
TD1728 □ □

Circuit Type

Package
Q:TDFN

Packing:
Blank：Tube
R:Type and Reel

Functional Block Diagram



Functional Block Diagram of TD1728

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
	All Other Pins (POK, OCSET, EN, FB, and RF to GND)	-0.3 ~ V_{CC}+0.3	V
	UGATE Voltage (UGATE to PHASE)<400ns Pulse Width>400ns Pulse Width	-5 ~ V_{BOOT}+0.3 -0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND)<400ns Pulse Width>400ns Pulse Width	-5 ~ V_{CC}+0.3 -0.3 ~ V_{CC}+0.3	V
V_{PHASE}	PHASE Voltage (PHASE to GND)<400ns Pulse Width>400ns Pulse Width	-5 ~ 35 -1 ~ 32	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	260	°C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	1.8 ~32	V
VCC	VCC Supply Voltage	4.5 ~ 5.5	V
V_{OUT}	Converter Output Voltage	0.7 ~ 5.5	V
I_{OUT}	Converter Output Current	~ 25	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note: Refer to the typical application circuit.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θJA	Thermal Resistance-Junction to Ambient 3mmx3mm TDFN-10	55	°C/W

Note: θ_{JA} is measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{CC} = 12V, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	TD1728			Unit
			Min.	Typ.	Max.	
VOUT AND VFB VOLTAGE						
V_{OUT}	Output Voltage	Adjustable output range	0.7	-	5.5	V
V_{REF}	Reference Voltage		-	0.7	-	V
	Regulation Accuracy	T_A = 25 °C	-0.5	-	+0.5	%
		T_A = 0 °C ~ 85 °C	-0.8	-	+0.8	%
		T_A = -40 °C ~ 85 °C	-1.0	-	+1.0	%
I_{FB}	FB Input Bias Current	FB = 0.7V	-	0.02	0.1	uA
T_{DIS}	V_{OUT} Discharge Time	EN low to FB = 0V	-	12	-	ms
SUPPLY CURRENT						
I_{VCC}	VCC Input Bias Current	VCC Current, PWM, EN = 5V, VFB = 0.735V, PHASE =	-	250	520	uA
I_{VCC_SHDN}	VCC Shutdown Current	EN = GND, VCC = 5V	-	0	1	uA
SWITCHING FREQUENCY AND SUTY AND INTERNAL SOFT-START						
F_{SW}	Switching Frequency	R_{RF} = 470k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	266	290	314	kHz
		R_{RF} = 200k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	312	340	368	
		R_{RF} = 100k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	349	380	411	
		R_{RF} = 39k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	395	430	465	
$T_{ON(MIN)}$	Minimum On Time		80	110	140	ns
$T_{OFF(MIN)}$	Minimum Off Time	V_{FB} = 0.65V, V_{PHASE} = -0.1V, OCSET = OPEN	350	450	550	ns
T_{SS}	Internal Soft-Start Time	EN High to V_{OUT} Regulation (95%)	0.7	1.0	1.3	ms
GATE DRIVER						
	UGATE Pull-Up Resistance	BOOT-UGATE = 0.5V	-	1.5	3	Ω
	UGATE Sink Resistance	UGATE-PHASE = 0.5V	-	0.7	1.8	Ω
	LGATE Pull-Up Resistance	PVCC-LGATE = 0.5V	-	1.0	2.2	Ω
	LGATE Sink Resistance	LGATE-GND = 0.5V	-	0.5	1.2	Ω
	UGATE to LGATE Dead-Time	UGATE falling to LGATE rising	-	20	-	ns
	LGATE to UGATE Dead-Time	LGATE falling to UGATE rising	-	20	-	ns
BOOTSTRAP SWITCH						
V_F	Ron	V_{VCC} - $V_{BOOT-GND}$, I_F = 10mA	-	0.5	0.8	V
I_R	Reverse Leakage	$V_{BOOT-GND}$ = 30V, V_{PHASE} = 25V, V_{VCC} = 5V	-	-	0.5	uA
VCC POR THRESHOLD						
V_{VCC_THR}	Rising VSS POR Threshold		4.2	4.35	4.45	V
	VCC POR Hysteresis		-	100	-	mV
CONTROL INPUTS						
	EN Voltage Threshold	Enable	1.8	-	-	V
		Shutdown	-	-	0.5	V

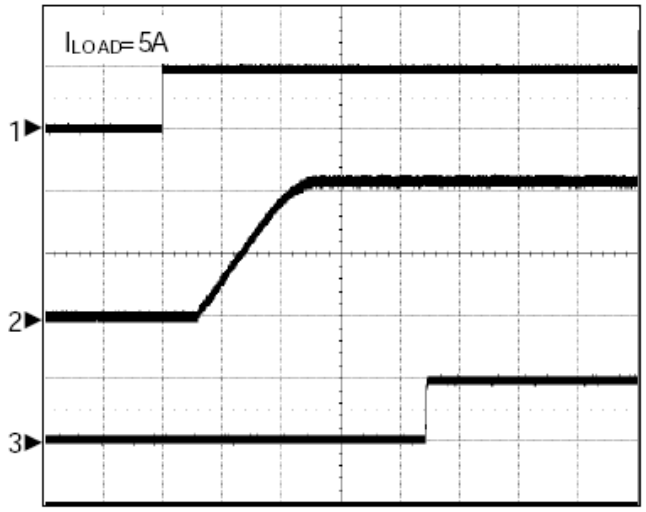
Electrical Characteristics(Cont.)

Symbol	Parameter	Test Conditions	T			Unit
			Min.	Typ.	Max.	
CONTROL INPUTS (CONT.)						
	EN Leakage	EN = 0V	-	0.1	1.0	uA
	RF Setting Threshold	Forced PWM Mode	1.8	-	-	V
		PFM/PWM Auto Skip Mode	-	-	0.5	V
POWER-OK INDICATOR						
V_{POK}	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%
		POK Low Hysteresis (POK Goes Low)	-	3	-	%
		POK out from Normal (POK Goes Low)	120	125	130	%
I_{POK}	POK Leakage Current	V_{POK} = 5V	-	0.1	1.0	uA
	POK Sink Current	V_{POK} = 0.5V	2.5	7.5	-	mA
	POK Enable Delay Time	EN High to POK High	1.4	2.0	2.6	ms
CURRENT SENSE						
I_{OCSET}	I_{OCSET} OCP Threshold	I_{OCSET} Sourcing	9	10	11	uA
$T_{CIOCSET}$	I_{OCSET} Temperature Coefficient	On The Basis of 25℃	-	4500	-	ppm/℃
V_{ROCSET}	Current-Limit Threshold Setting Range	$V_{OCSET-GND}$ Voltage, Over All Temperature	0.24	-	1.6	V
	Over Current-Limit	($V_{OCSET-GND}$-$V_{GND-PHASE}$) Voltage, $V_{OCSET-GND}$=60mV	-10	0	10	mV
	Zero Crossing Comparator	$V_{GND-PHASE}$ Voltage, EN=3.3V	-9.5	0.5	10.5	mV
PROTECTION						
V_{UV}	UVP Threshold		60	70	80	%
	UVP Hysteresis		-	3	-	%
	UVP Debounce Interval		-	16	-	us
	UVP Enable Delay	EN High to UVP Workable	1.4	2	2.6	ms
V_{OVR}	OVP Rising Threshold		120	125	130	%
	OVP Propagation Delay	V_{FB} Rising, DV=10mV	-	1.5	-	us
T_{OTR}	OTP Rising Threshold (Note 4)		-	140	-	℃
	OTP Hysteresis (Note 4)		-	25	-	℃

Note : Guaranteed by design, not production tested.

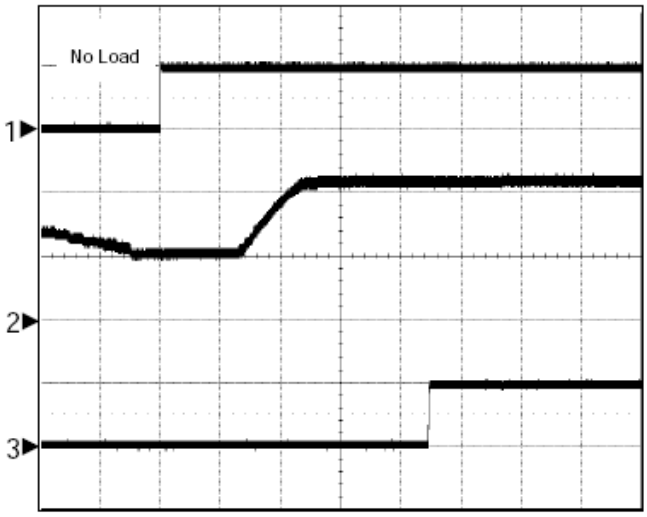
Typical Operating Characteristics

Enable at Zero Initial Voltage of V_{OUT}



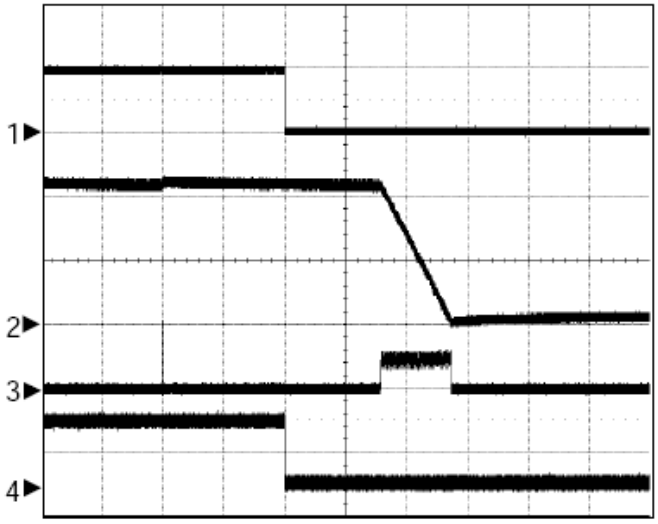
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 500μs/Div

Enable Before End of Soft-Stop



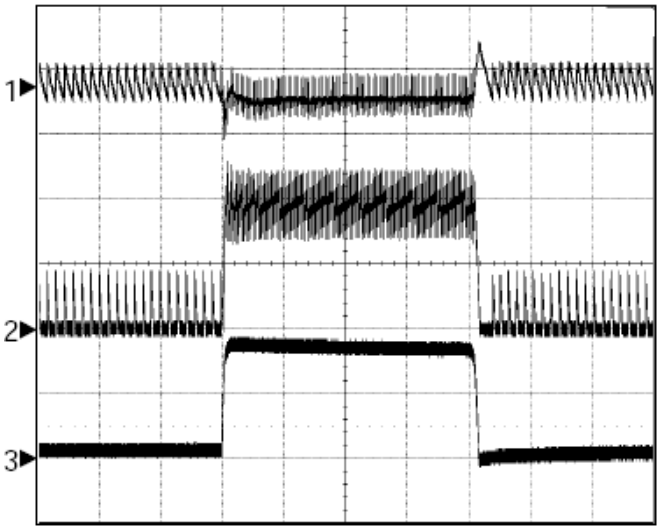
CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{POK}, 5V/Div, DC
TIME: 500μs/Div

Shutdown with Soft-Stop at No Load



CH1: V_{EN}, 5V/Div, DC
CH2: V_{OUT}, 500mV/Div, DC
CH3: V_{LGATE}, 5V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 5ms/Div

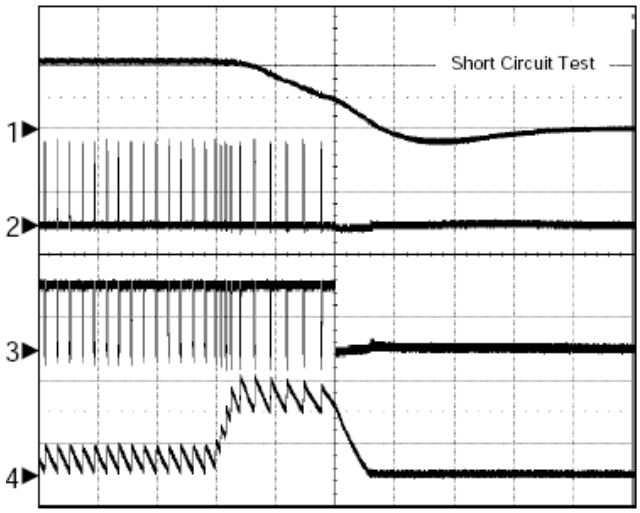
VOUT=1.1V, Load Transient 1A->18A->1A



CH1: V_{OUT}, 50mV/Div, AC
CH2: I_L, 10A/Div, DC
CH3: I_{OUT}, 10A/Div, DC
TIME: 100μs/Div

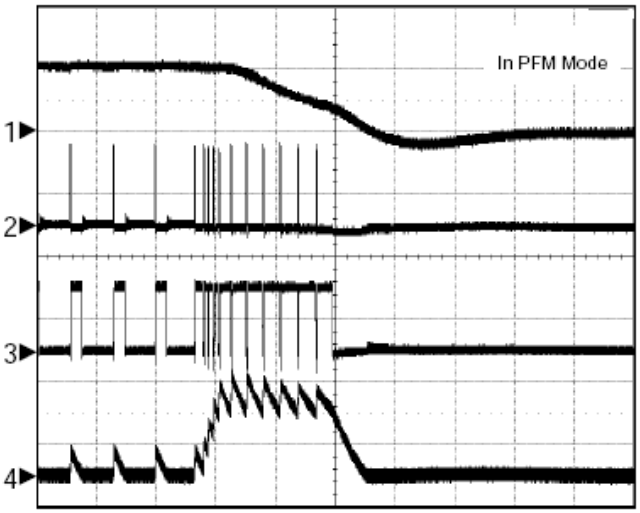
Typical Operating Characteristics(Cont.)

Under-Voltage Protection



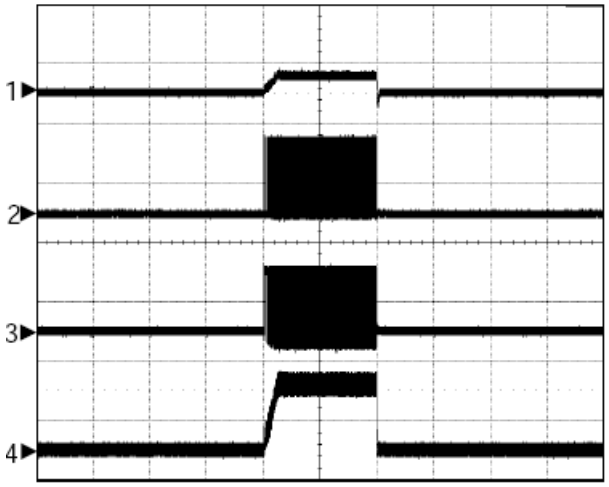
CH1: V_{OUT}, 1V/Div, DC
CH2: V_{UGATE}, 20V/Div, DC
CH3: V_{LGATE}, 5V/Div, DC
CH4: I_L, 20A/Div, DC
TIME: 20μs/Div

Short Circuit Test



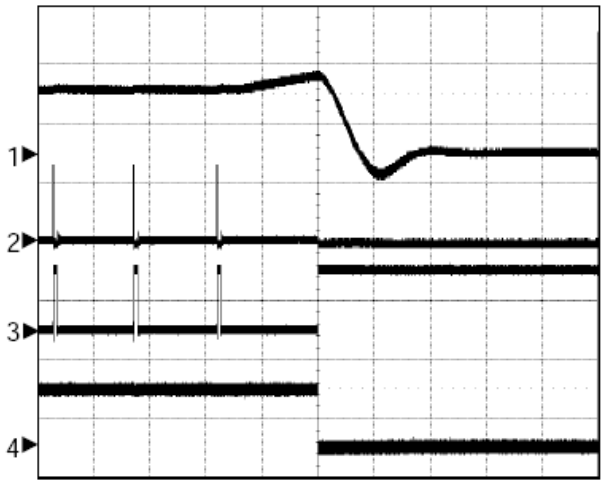
CH1: V_{OUT}, 1V/Div, DC
CH2: V_{UGATE}, 20V/Div, DC
CH3: V_{LGATE}, 5V/Div, DC
CH4: I_L, 20A/Div, DC
TIME: 20μs/Div

Power On in Short Circuit



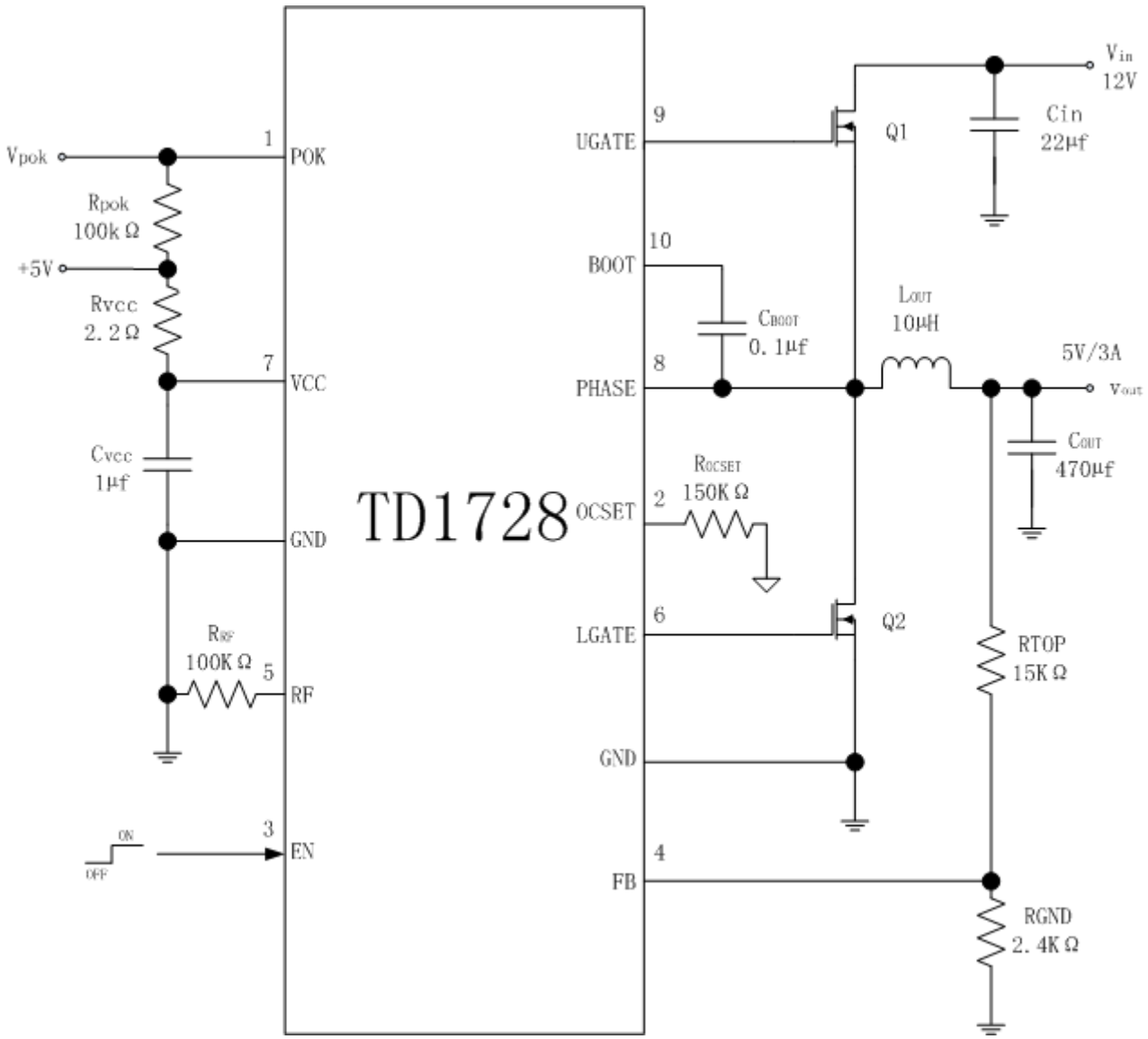
CH1: V_{OUT}, 1V/Div, DC
CH2: V_{UGATE}, 20V/Div, DC
CH3: V_{LGATE}, 5V/Div, DC
CH4: I_L, 20A/Div, DC
TIME: 1ms/Div

Over-Voltage Protection



CH1: V_{OUT}, 1V/Div, DC
CH2: V_{UGATE}, 20V/Div, DC
CH3: V_{LGATE}, 5V/Div, DC
CH4: V_{POK}, 5V/Div, DC
TIME: 50μs/Div

Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudofixed requency with input voltage feed-forward. This architecture elies on the output filter capacitor's effective series esistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal.In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a oneshot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.

The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage,output current, and temperature. Both in PFM and PWM,the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (450ns,typical). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time oneshot has timed out.

Pulse-Frequency Modulation (PFM)

When VRF is below the RF low threshold (0.5V, maximum),the converter is in automatic PFM/PWM operation mode.In PFM mode, an automatic switchover to pulse-frequencymodulation (PFM) takes place at light loads. Thisswitchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point).The on-time of PFM is given by:

$$T_{ON\text{-}PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON\text{-}PFM} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Forced-PWM Mode

The RF pin should be pulled high to POK and the converter is in forced-PWM operation mode. The Forced-PWM mode disables the zero-crossing comparator, which truncates the low-side switch on-time at the inductor current zero crossing. This causes the low-side gate-drive waveform to become the complement of the high-side gatedrive waveform. This in turn causes the inductor current to reverse at light loads while UGATE maintains a duty factor of VOUT/VIN. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced-PWM mode is the most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising VCC POR Threshold (4.35V, typical), the POR signal goes high and the chip initiates soft-start operations. There is almost no hysteresis to POR voltage threshold (about 100mV typical). When VCC voltage drops lower than 4.25V (typical), the POR disables the chip.

EN Pin Control

When VEN is above the EN high threshold (1.8V, typical), the converter is enabled. When VEN is below the EN low threshold (0.5V, typical), the chip is in the shutdown and only low leakage current is taken from VCC.

Digital Soft-Start

The TD1728 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during softstart process. The figure 1 shows soft-start sequence.When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to rampup the output voltage. The soft-start interval is 1ms (typical)and independent of the UGATE

Function Description(Cont.)

switching frequency.

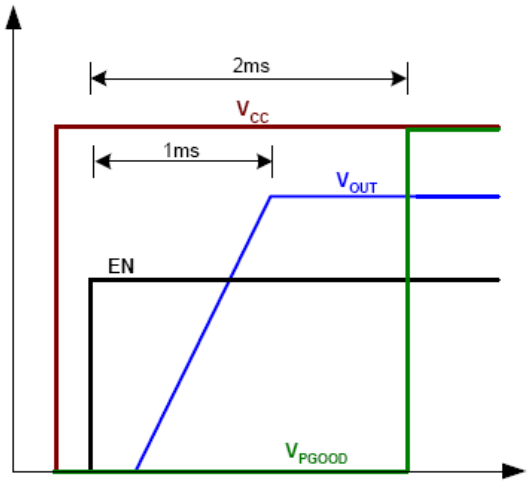


Figure 1. Soft-Start Sequence

During soft-start stage before the PGOOD pin is ready,the under-voltage protection is prohibited. The over-voltage and current-limit protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the internal digital soft-start voltage equals to the VFB voltage. This will ensure that the output voltage starts from its existing voltage level.In the event of under-voltage, over-temperature, or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltage to the GND. The duration of the discharge time is 8ms.

Power OK Indicator

The TD1728 features an open-drain POK pin to indicate output regulation status. In normal operation, when the output voltage rises 90% of its target value, the POK goes high after 63us internal delay. When the output voltage outruns 70% or 125% of the target voltage, POK signal will be pulled low immediately.

Since the FB pin is used for both feedback and monitoring purposes, the output voltage deviation can be coupled directly to the FB pin by the capacitor in parallel with the voltage divider as shown in the typical applications. In order to prevent false POK from dropping, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The undervoltage protection circuit continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the undervoltage threshold, the under-voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 16μs debounce time, the device turns off both high-side and low-side MOSEFET with latched and starts a soft-stop process to shut down the output gradually. Toggling enable pin to low or recycling VCC,will clear the latch and bring the chip back to operation.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator designed with a 1.5μs noise filter will force the lowside MOSFET gate driver fully turn on and latch high. This action actively pulls down the output voltage.This OVP scheme only clamps the voltage overshoot and does not invert the output voltage when otherwise activated with a continuously high output from low-side

Over-Voltage Protection (OVP) (Cont.)

MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can only be reset by toggling EN, VCC power-on-reset signal.

Current-Limit

The current-limit circuit employs a "valley" current-sensing algorithm (See Figure 2). The TD1728 uses the low-side MOSFET's RDS(ON) of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the currentlimit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the currentlimit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage

Function Description(Cont.)

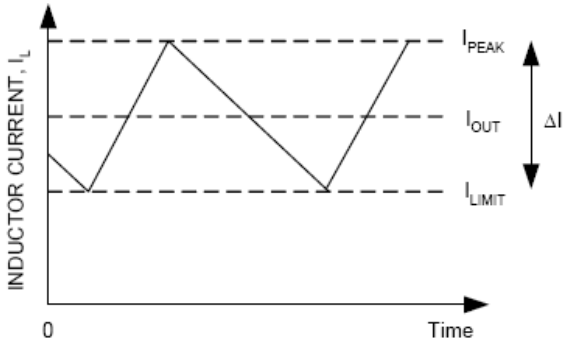


Figure 2. Current-Limit Algorithm

The PWM controller uses the low-side MOSFETs on-resistance RDS(ON) to monitor the current for protection against shortened outputs. The MOSFET's RDS(ON) is varied by temperature and gate to source voltage, the user should determine the maximum RDS(ON) in manufacture's datasheet.

The OCSET pin can source 10μA through an external resistor for adjusting current-limit threshold. The voltage at OCSET pin is equal to 10μA x ROCSET. The relationship between the sampled voltage VOCSET and the current-limit threshold ILIMIT is given by:

$$\frac{1}{8} \times 10\,\mu A \times R_{OCSET} = I_{LIMIT} \times R_{DS(ON)}$$

Where ROCSET is the resistor of current-limit setting threshold. RDS(ON) is the low side MOSFETs conducive resistance. ILIMIT is the setting current-limit threshold. ILIMIT can be expressed as IOUT minus half of peak-to-peak inductor current.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance.

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature TOTR, the IC will enter the overtemperature protection state that suspends the PWM,which forces the UGATE and LGATE gate drivers outputlow. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 25oC. The OTP is designed with a 25oC hysteresis to lower the average TJ during continuous thermal overload conditions, which increases lifetime of the TD1728.

Programming the On-Time Control and PWM Switching Frequency

The TD1728 does not use a clock signal to produce PWM. The device uses the constant-on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage VOUT and inverses proportional to input voltage VIN. The switching frequency is selectable from four preset values by a resistor connected to RF pin as shown in Table1.

TD1728 doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring VPHASE voltage as input voltage to calculate on-time when the high-side MOSFET is turned on. And then, use the relationship between ontime and duty cycle to obtain the switching frequency.

Table 1.

Resistance R_{RF} (kΩ)	Switching Frequency F_{sw} (kHz)
470	290
200	340
100	380
39	430

Application Information

Output Voltage Setting

The output voltage is adjustable from 0.7V to 5.5V with a resistor-divider connected with FB, GND, and converter's output. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by:

$$V_{OUT} = 0.7 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where 0.7 is the reference voltage, RTOP is the resistor connected from converter's output to FB, and RGND is the resistor connected from FB to GND. Suggested RGND is in the range from 1k to 20kΩ. To prevent stray pickup, locate resistors RTOP and RGND close to TD1728.

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, IRIPPLE, and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the switching frequency of the regulator.Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulatorload transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (FSW) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor which is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors which have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turnoff,the output voltage ripple includes the capacitance voltage drop ΔVCOUT and ESR voltage drop ΔVESR caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1μF) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately IOUT/2,where IOUT is the load current. During power-up, the input capacitors have to handle great amount of surge current.For low-duty notebook appliactions, ceramic capacitor is recommended. The

Application Information(Cont.)

capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the RDS(ON) of the MOSFET:

For the low-side MOSFET, before it is turned on, the body diode has been conducting. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the lowside MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, when using smaller RDS(ON) of the low-side MOSFET, the converter can reduce power loss. The gate charge for this MOSFET is usually the secondary consideration.

The high-side MOSFET does not have this zero voltage switching condition; in addition, because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gatedriver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement.

The losses in the MOSFETs have two components:conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$
$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where

IOUT is the load current

TC is the temperature dependency of RDS(ON)

FSW is the switching frequency

tSW is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss.The switching interval, tSW, is the function of the reverse transfer capacitance CRSS. The (1+TC) term is a factor in the temperature dependency of the RDS(ON) and can be extracted from the “RDS(ON) vs. Temperature” curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator.With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off,current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

·Keep the switching nodes (UGATE, LGATE, BOOT,and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals.Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.

·The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.

·Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible.Minimizing the impedance with wide

Application Information(Cont.)

layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (VIN and PHASE nodes) can get better heat sinking.

·The GND is the current sensing circuit reference ground and also the power ground of the LGATE lowside MOSFET. On the other hand, the GND trace should be a separate trace and independently go to the source of the low-side MOSFET. Besides, the current sense resistor should be close to OCSET pin to avoid parasitic capacitor effect and noise coupling.

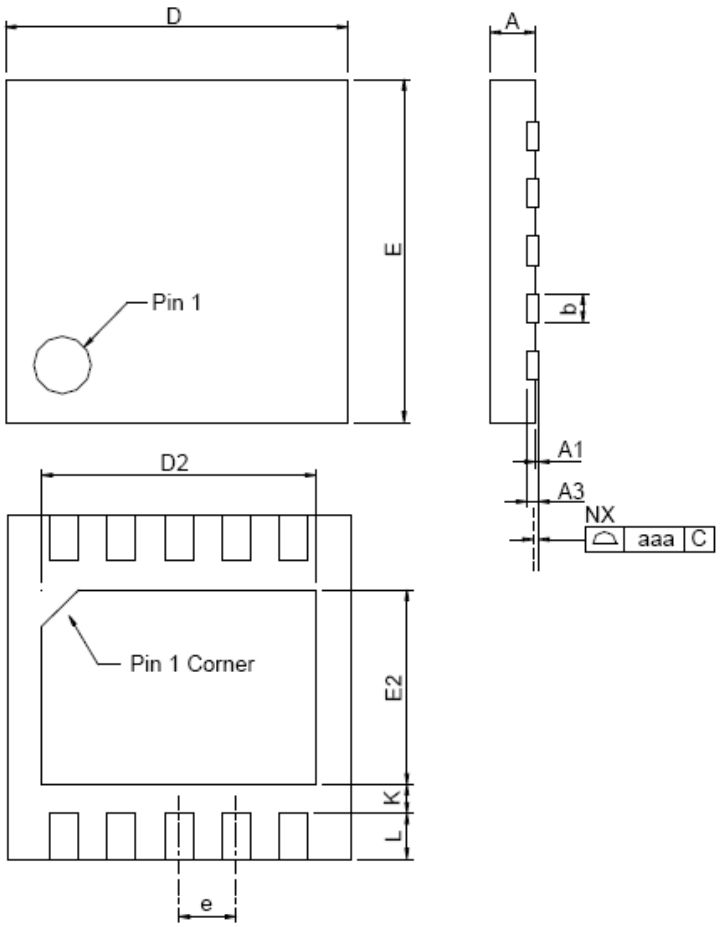
·Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example,place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible.)

·The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.

·Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces(UGATE, LGATE, BOOT, and PHASE).

Package Information

TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Design Notes

High-Performance PWM Controller TD1730

General Description

The TD1730 is a single-phase, constant-on-time, synchronous PWM controller, which drives N-channel MOSFETs. The TD1730 steps down high voltage to generate low-voltage chipset or RAM supplies in notebook computers.

The TD1730 provides excellent transient response and accurate DC voltage output in either PFM or PWM Mode. In Pulse Frequency Mode (PFM), the TD1730 provides very high efficiency over light to heavy loads with loading- modulated switching frequencies. In PWM Mode, the converter works nearly at constant frequency for low-noise requirements.

The TD1730 is equipped with accurate positive current- limit, output under-voltage, and output over-voltage protections, perfect for NB applications. The Power-On-Reset function monitors the voltage on VCC to prevent wrong operation during power-on. The TD1730 has a 1ms digital soft-start and built-in an integrated output discharge method for soft-stop. An internal integrated soft-start ramps up the output voltage with programmable slew rate to reduce the start-up current. A soft-stop function actively discharges the output capacitors with controlled reverse inductor current.

The TD1730 is available in 10pin TDFN 3x3 package.

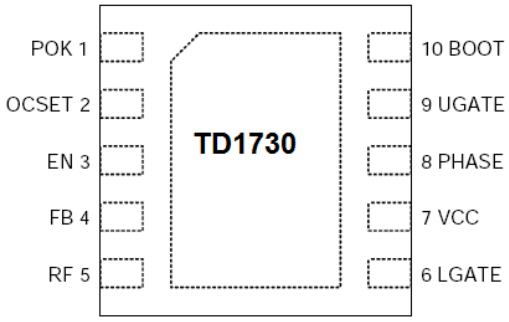
Features

- Adjustable Output Voltage from +0.7V to +5.5V
- 0.7V Reference Voltage
- ±1% Accuracy Over-Temperature
- Operates from an Input Battery Voltage Range of +1.8V to +32V
- Power-On-Reset Monitoring on VCC Pin
- Excellent Line and Load Transient Responses
- PFM Mode for Increased Light Load Efficiency
- Selectable PWM Frequency from 4 Preset Values
- Integrated MOSFET Drivers
- Integrated Bootstrap Forward P-CH MOSFET
- Adjustable Integrated Soft-Start and Soft-Stop
- Selectable Forced PWM or Automatic PFM/PWM Mode
- Power Good Monitoring
- 70% Under-Voltage Protection
- 125% Over-Voltage Protection
- Adjustable Current-Limit Protection
- Using Sense Low-Side MOSFET's $R_{DS(ON)}$
- Over-Temperature Protection
- Auto Rework from Protection Mode
- TDFN-10 3x3 Package
- Lead Free and Green Devices Available (RoHS Compliant)

Applications

- Notebook
- Table PC
- Hand-Held Portable
- AIO PC
- LCD Monitor / TV
- Battery Charger
- ADSL Modem
- Telecom / Networking Equipment

Pin Assignments



TDFN3x3-10
Top View

= GND and Thermal Pad (connected to GND plane for better heat dissipation)

PIN		NAME	FUNCTION
NO.			
TDFN3x3	TDFN2x2		
1	1	POK	Power Good Output. POK is an open drain output used to indicate the status of the output voltage. Connect the POK in to +5V through a pull-high resistor.
2	2	OCSET	Current-Limit Threshold Setting Pin. There is an internal source current 10 uA through a resistor from OCSET pin to GND. This pin is used to monitor the voltage drop across the Drain and Source of the low-side MOSFET for current-limit.
3	3	EN	Enable Pin of The PWM Controller. When the EN is above enable logic level, the Device is workable. When the EN is below shutdown logic level, the device is in shutdown and only low leakage current is taken from V_{CC} and V_{IN}.
4	4	FB	Output Voltage Feedback Pin. This pin is connected to the resistive divider that set the desired output voltage. The POK, UVP, and OVP circuits detect this signal to report output voltage status.
5	-	RF	This Pin is Allowed to Adjust The Switching Frequency. Connect a resistor R_{RF} to set switching frequency as show in Table1. The pin also controls forced PWM mode or PFM/PWM auto skip mode selection. When RF pin is pulled down to GND, the device is in automatic PFM/PWM Mode. When RF pin is pulled high to POK, the device is in force PWM mode.
6	6	LGATE	Output of The Low-side MOSFET Driver. Connect this pin to Gate of the low-side MOSFET. Swings from GND to VCC.
7	7	VCC	Supply Voltage Input Pin for Control Circuitry. Connect +5V from the VCC pin to the GND pin. Decoupling at least 1u F of a MLCC capacitor from the VCC pin to the GND pin.
8	8	PHASE	Junction Point of The High-side MOSFET Source, Output Filter Inductor and The Low-side MOSFET Drain. Connect this pin to the Source of the high-side MOSFET. PHASE serves as the lower supply rail for the UGATE high-side gate driver.
9	9	UGATE	Output of The High-side MOSFET Driver. Connect this pin to Gate of the high-side MOSFET.
10	10	BOOT	Supply Input for The UGATE Gate Driver and An Internal Level-shift Circuit. Connect to an external capacitor to create a boosted voltage suitable to drive a logic-level N-channel MOSFET.
Exposed Pad	5	GND	Signal Ground for The IC

Ordering Information

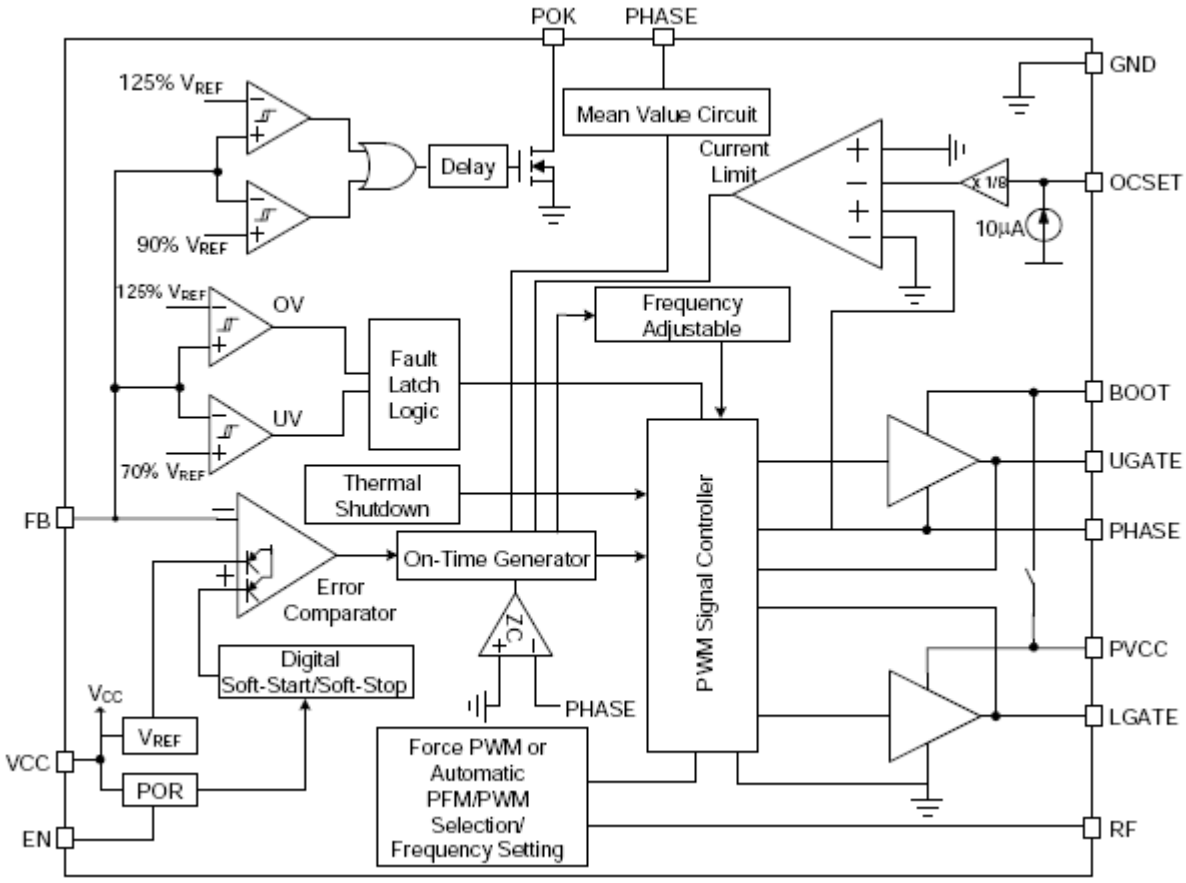
TD1730 □ □

Circuit Type

Package
Q:TDFN

Packing:
Blank：Tube
R:Type and Reel

Functional Block Diagram



Functional Block Diagram of TD1730

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{CC}	VCC Supply Voltage (VCC to GND)	-0.3 ~ 7	V
$V_{BOOT-GND}$	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 35	V
V_{BOOT}	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 7	V
	All Other Pins (POK, OCSET, EN, FB, and RF to GND)	-0.3 ~ V_{CC}+0.3	V
	UGATE Voltage (UGATE to PHASE) Pulse Width <400ns	-5 ~ V_{BOOT}+0.3	
	Pulse Width>400ns	-0.3 ~ V_{BOOT}+0.3	V
	LGATE Voltage (LGATE to GND) Pulse Width <400ns	-5 ~ V_{CC}+0.3	
	Pulse Width>400ns	-0.3 ~ V_{CC}+0.3	V
	PHASE Voltage (PHASE to GND) Pulse Width <400ns	-5 ~ 35	
V_{PHASE}	Pulse Width>400ns	-1 ~ 32	V
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature	-65 ~ 150	°C
T_{SDR}	Maximum Soldering Temperature, 10 Seconds	260	°C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Recommended Operating Conditions

Symbol	Parameter	Range	Unit
V_{IN}	Converter Input Voltage	1.8 ~32	V
VCC	VCC Supply Voltage	4.5 ~ 5.5	V
V_{OUT}	Converter Output Voltage	0.7 ~ 5.5	V
I_{OUT}	Converter Output Current	~ 25	A
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note: Refer to the typical application circuit.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θJA	Thermal Resistance-Junction to Ambient 3mmx3mm TDFN-10	55	°C/W

Note: θ_{JA} is measured with the component mounted on a high effective the thermal conductivity test board in free air. The exposed pad of package is soldered directly on the PCB.

Electrical Characteristics

Refer to the typical application circuit. These specifications apply over V_{CC} = 12V, T_A = -40°C to 85°C, unless otherwise noted. Typical values are at T_A = 25°C.

Symbol	Parameter	Test Conditions	TD1730			Unit
			Min.	Typ.	Max.	
VOUT AND VFB VOLTAGE						
V_{OUT}	Output Voltage	Adjustable output range	0.7	-	5.5	V
V_{REF}	Reference Voltage		-	0.7	-	V
	Regulation Accuracy	T_A = 25 °C	-0.5	-	+0.5	%
		T_A = 0 °C ~ 85 °C	-0.8	-	+0.8	%
		T_A = -40 °C ~ 85 °C	-1.0	-	+1.0	%
I_{FB}	FB Input Bias Current	FB = 0.7V	-	0.02	0.1	uA
T_{DIS}	V_{OUT} Discharge Time	EN low to FB = 0V	-	12	-	ms
SUPPLY CURRENT						
I_{VCC}	VCC Input Bias Current	VCC Current, PWM, EN = 5V, VFB = 0.735V, PHASE =	-	250	520	uA
I_{VCC_SHDN}	VCC Shutdown Current	EN = GND, VCC = 5V	-	0	1	uA
SWITCHING FREQUENCY AND SUTY AND INTERNAL SOFT-START						
F_{SW}	Switching Frequency	R_{RF} = 470k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	115	135	155	kHz
		R_{RF} = 200k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	140	165	180	
		R_{RF} = 100k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	155	185	215	
		R_{RF} = 39k , T_A = 25°C, V_{IN}=8V, V_{OUT}=1.1V, I_{OUT}=10A	185	215	245	
$T_{ON(MIN)}$	Minimum On Time		80	110	140	ns
$T_{OFF(MIN)}$	Minimum Off Time	V_{FB} = 0.65V, V_{PHASE} = -0.1V, OCSET = OPEN	350	450	550	ns
T_{SS}	Internal Soft-Start Time	EN High to V_{OUT} Regulation (95%)	0.7	1.0	1.3	ms
GATE DRIVER						
	UGATE Pull-Up Resistance	BOOT-UGATE = 0.5V	-	1.5	3	Ω
	UGATE Sink Resistance	UGATE-PHASE = 0.5V	-	0.7	1.8	Ω
	LGATE Pull-Up Resistance	PVCC-LGATE = 0.5V	-	1.0	2.2	Ω
	LGATE Sink Resistance	LGATE-GND = 0.5V	-	0.5	1.2	Ω
	UGATE to LGATE Dead-Time	UGATE falling to LGATE rising	-	20	-	ns
	LGATE to UGATE Dead-Time	LGATE falling to UGATE rising	-	20	-	ns
BOOTSTRAP SWITCH						
V_F	Ron	V_{VCC} - $V_{BOOT-GND}$, I_F = 10mA	-	0.5	0.8	V
I_R	Reverse Leakage	$V_{BOOT-GND}$ = 30V, V_{PHASE} = 25V, V_{VCC} = 5V	-	-	0.5	uA
VCC POR THRESHOLD						
V_{VCC_THR}	Rising VSS POR Threshold		4.2	4.35	4.45	V
	VCC POR Hysteresis		-	100	-	mV
CONTROL INPUTS						
	EN Voltage Threshold	Enable	1.8	-	-	V
		Shutdown	-	-	0.5	V

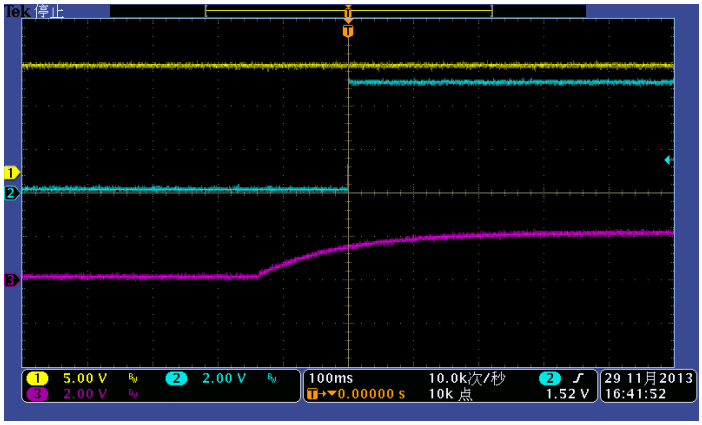
Electrical Characteristics(Cont.)

Symbol	Parameter	Test Conditions	T			Unit
			Min.	Typ.	Max.	
CONTROL INPUTS (CONT.)						
	EN Leakage	EN = 0V	-	0.1	1.0	uA
	RF Setting Threshold	Forced PWM Mode	1.8	-	-	V
		PFM/PWM Auto Skip Mode	-	-	0.5	V
POWER-OK INDICATOR						
V_{POK}	POK Threshold	POK in from Lower (POK Goes High)	87	90	93	%
		POK Low Hysteresis (POK Goes Low)	-	3	-	%
		POK out from Normal (POK Goes Low)	120	125	130	%
I_{POK}	POK Leakage Current	V_{POK} = 5V	-	0.1	1.0	uA
	POK Sink Current	V_{POK} = 0.5V	2.5	7.5	-	mA
	POK Enable Delay Time	EN High to POK High	1.4	2.0	2.6	ms
CURRENT SENSE						
I_{OCSET}	I_{OCSET} OCP Threshold	I_{OCSET} Sourcing	9	10	11	uA
$T_{CIOCSET}$	I_{OCSET} Temperature Coefficient	On The Basis of 25℃	-	4500	-	ppm/°
V_{ROCSET}	Current-Limit Threshold Setting Range	$V_{OCSET-GND}$ Voltage, Over All Temperature	0.24	-	1.6	V
	Over Current-Limit	($V_{OCSET-GND}$-$V_{GND-PHASE}$) Voltage, $V_{OCSET-GND}$=60mV	-10	0	10	mV
	Zero Crossing Comparator	$V_{GND-PHASE}$ Voltage, EN=3.3V	-9.5	0.5	10.5	mV
PROTECTION						
V_{UV}	UVP Threshold		60	70	80	%
	UVP Hysteresis		-	3	-	%
	UVP Debounce Interval		-	16	-	us
	UVP Enable Delay	EN High to UVP Workable	1.4	2	2.6	ms
V_{OVR}	OVP Rising Threshold		120	125	130	%
	OVP Propagation Delay	V_{FB} Rising, DV=10mV	-	1.5	-	us
T_{OTR}	OTP Rising Threshold (Note 4)		-	140	-	oC
	OTP Hysteresis (Note 4)		-	25	-	oC

Note : Guaranteed by design, not production tested.

Typical Operating Characteristics

Start with Vin-En No Load

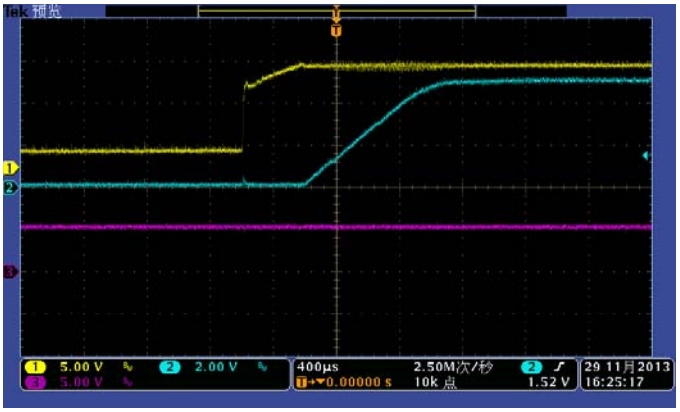


CH1，Vin

CH2，Vout

CH3，EN

Start with En-Vin No Load

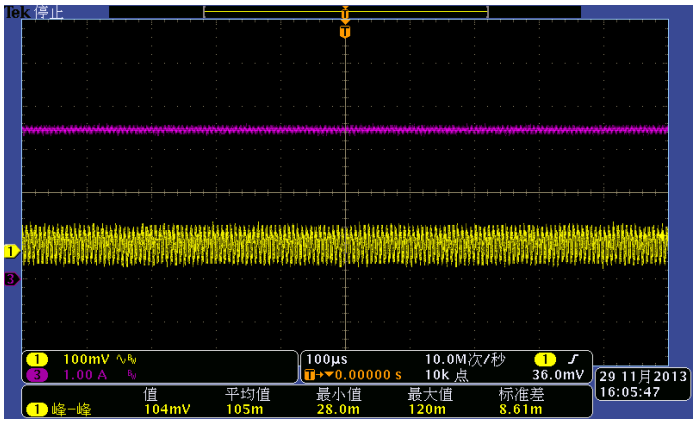


CH1，Vin

CH2，Vout

CH3，EN

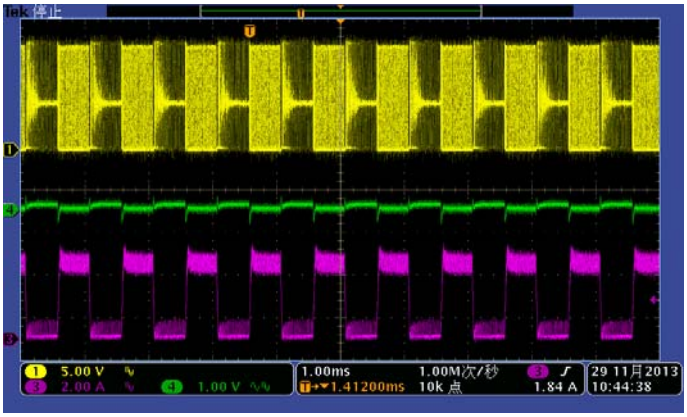
3.4A Load Ripple test



CH1，Vout

CH3，Iload

Load Transient 0.1A-3.4A



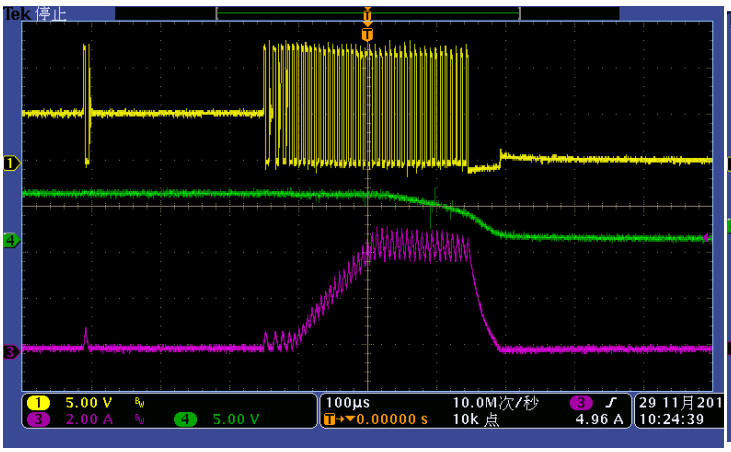
CH1，PHASE

CH3，Iload

CH4，Vout

Typical Operating Characteristics(Cont.)

Short Circuit Test

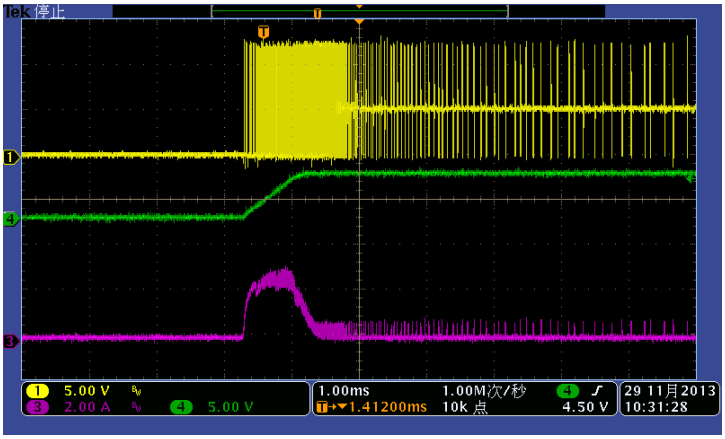


CH1，PHASE

CH3，Isw

CH4，Vout

Short Circuit recovery

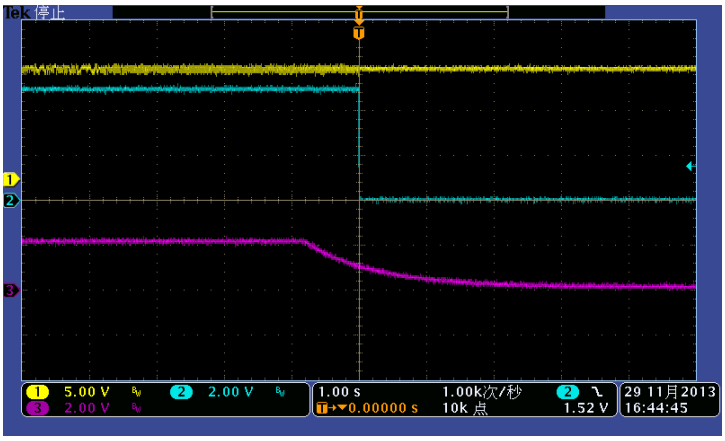


CH1，PHASE

CH3，Isw

CH4，Vout

Shurtdown with EN No Load

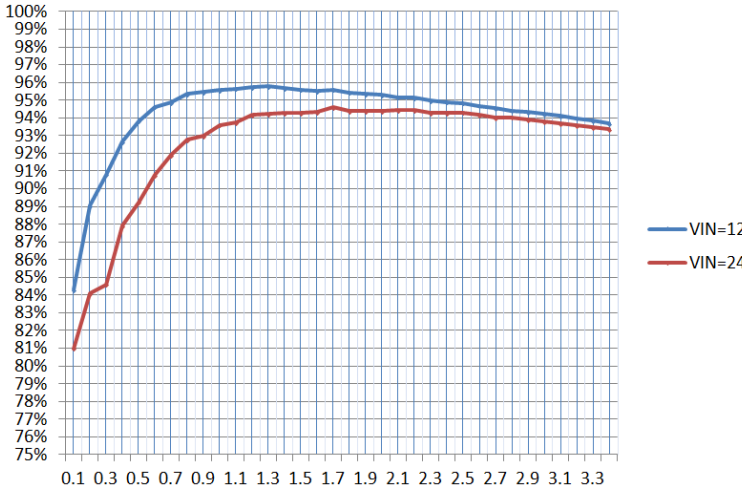


CH1，Vin

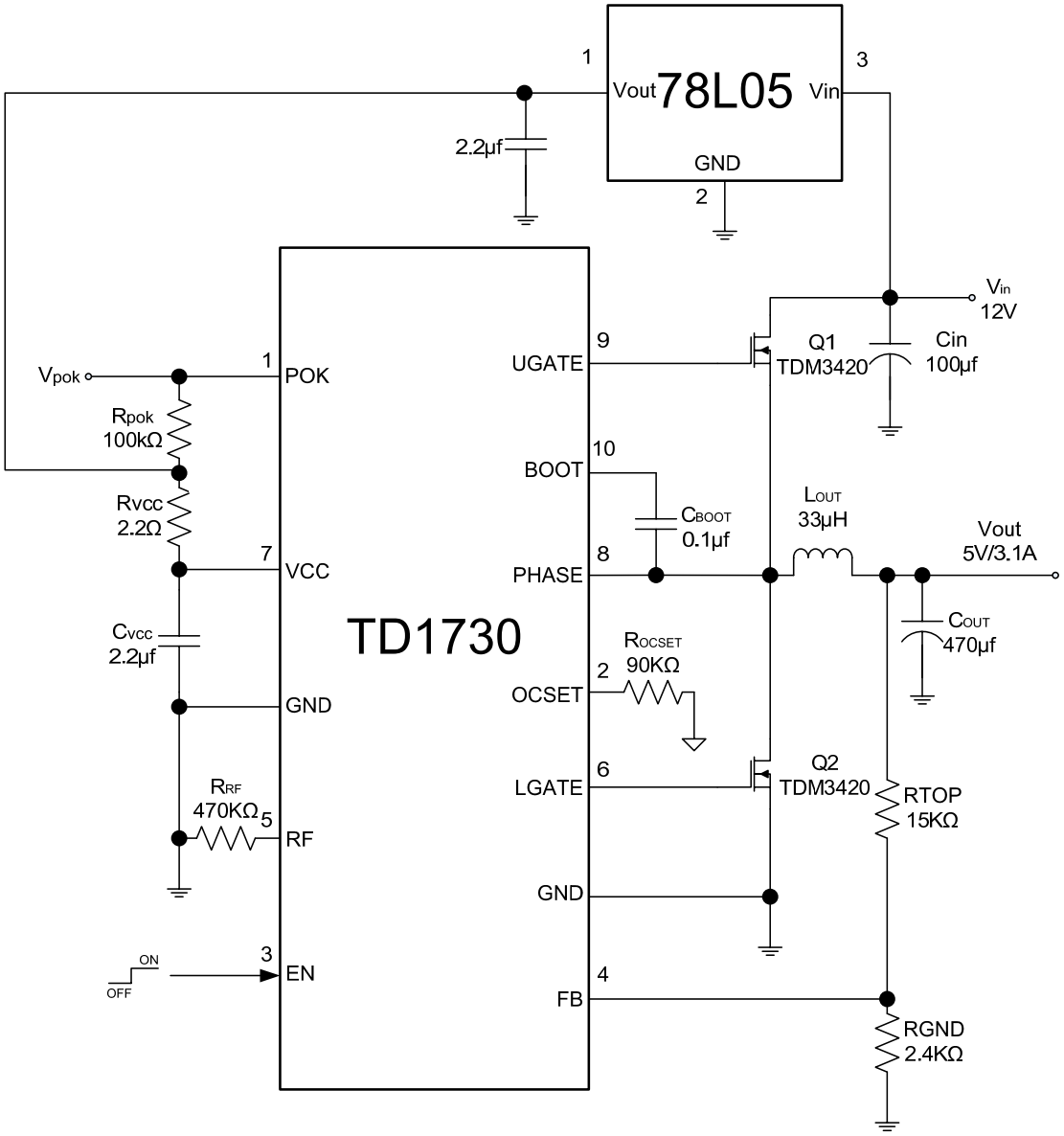
CH2，Vout

CH3，EN

Efficiency vs. Load



Typical Application Circuit



Function Description

Constant-On-Time PWM Controller with Input Feed-Forward

The constant-on-time control architecture is a pseudofixed requency with input voltage feed-forward. This architecture elies on the output filter capacitor's effective series esistance (ESR) to act as a current-sense resistor, so the output ripple voltage provides the PWM ramp signal.In PFM operation, the high-side switch on-time controlled by the on-time generator is determined solely by a oneshot whose pulse width is inversely proportional to input voltage and directly proportional to output voltage. In PWM operation, the high-side switch on-time is determined by a switching frequency control circuit in the on-time generator block.

The switching frequency control circuit senses the switching frequency of the high-side switch and keeps regulating it at a constant frequency in PWM mode. The design improves the frequency variation and is more outstanding than a conventional constant-on-time controller, which has large switching frequency variation over input voltage,output current, and temperature. Both in PFM and PWM,the on-time generator, which senses input voltage on PHASE pin, provides very fast on-time response to input line transients.

Another one-shot sets a minimum off-time (450ns,typical). The on-time one-shot is triggered if the error comparator is high, the low-side switch current is below the current-limit threshold, and the minimum off-time oneshot has timed out.

Pulse-Frequency Modulation (PFM)

When VRF is below the RF low threshold (0.5V, maximum),the converter is in automatic PFM/PWM operation mode.In PFM mode, an automatic switchover to pulse-frequencymodulation (PFM) takes place at light loads. Thisswitchover is affected by a comparator that truncates the low-side switch on-time at the inductor current zero crossing. This mechanism causes the threshold between PFM and PWM operation to coincide with the boundary between continuous and discontinuous inductor-current operation (also known as the critical conduction point).The on-time of PFM is given by:

$$T_{ON\text{-}PFM} = \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the nominal switching frequency of the converter in PWM mode.

The load current at handoff from PFM to PWM mode is given by:

$$I_{LOAD(PFM\ to\ PWM)} = \frac{1}{2} \times \frac{V_{IN} - V_{OUT}}{L} \times T_{ON\text{-}PFM} = \frac{V_{IN} - V_{OUT}}{2L} \times \frac{1}{F_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

Forced-PWM Mode

The RF pin should be pulled high to POK and the converter is in forced-PWM operation mode. The Forced-PWM mode disables the zero-crossing comparator, which truncates the low-side switch on-time at the inductor current zero crossing. This causes the low-side gate-drive waveform to become the complement of the high-side gatedrive waveform. This in turn causes the inductor current to reverse at light loads while UGATE maintains a duty factor of VOUT/VIN. The benefit of Forced-PWM mode is to keep the switching frequency fairly constant. The Forced-PWM mode is the most useful for reducing audio frequency noise, improving load-transient response, and providing sink-current capability for dynamic output voltage adjustment.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls when the VCC voltage is low. The POR function continually monitors the bias supply voltage on the VCC pin if at least one of the enable pins is set high. When the rising VCC voltage reaches the rising VCC POR Threshold (4.35V, typical), the POR signal goes high and the chip initiates soft-start operations. There is almost no hysteresis to POR voltage threshold (about 100mV typical). When VCC voltage drops lower than 4.25V (typical), the POR disables the chip.

EN Pin Control

When VEN is above the EN high threshold (1.8V, typical), the converter is enabled. When VEN is below the EN low threshold (0.5V, typical), the chip is in the shutdown and only low leakage current is taken from VCC.

Digital Soft-Start

The TD1730 integrates digital soft-start circuits to ramp up the output voltage of the converter to the programmed regulation setpoint at a predictable slew rate. The slew rate of output voltage is internally controlled to limit the inrush current through the output capacitors during softstart process. The figure 1 shows soft-start sequence.When the EN pin is pulled above the rising EN threshold voltage, the device initiates a soft-start process to rampup the output voltage. The soft-start interval is 1ms (typical)and independent of the UGATE

Function Description(Cont.)

switching frequency.

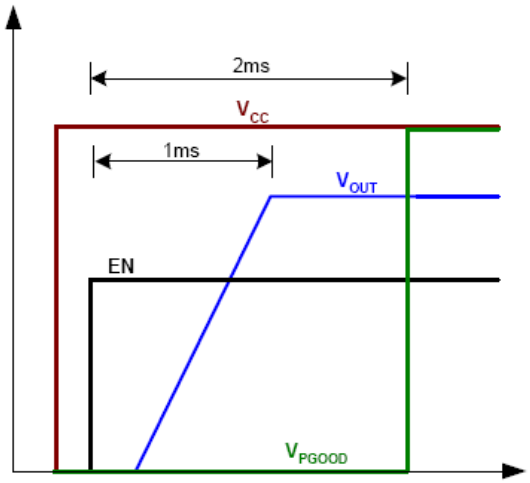


Figure 1. Soft-Start Sequence

During soft-start stage before the PGOOD pin is ready,the under-voltage protection is prohibited. The over-voltage and current-limit protection functions are enabled. If the output capacitor has residue voltage before start-up, both low-side and high-side MOSFETs are in off-state until the internal digital soft-start voltage equals to the VFB voltage. This will ensure that the output voltage starts from its existing voltage level.In the event of under-voltage, over-temperature, or shutdown, the chip enables the soft-stop function. The soft-stop function discharges the output voltage to the GND. The duration of the discharge time is 8ms.

Power OK Indicator

The TD1730 features an open-drain POK pin to indicate output regulation status. In normal operation, when the output voltage rises 90% of its target value, the POK goes high after 63us internal delay. When the output voltage outruns 70% or 125% of the target voltage, POK signal will be pulled low immediately.

Since the FB pin is used for both feedback and monitoring purposes, the output voltage deviation can be coupled directly to the FB pin by the capacitor in parallel with the voltage divider as shown in the typical applications. In order to prevent false POK from dropping, capacitors need to parallel at the output to confine the voltage deviation with severe load step transient.

Under-Voltage Protection (UVP)

In the operational process, if a short-circuit occurs, the output voltage will drop quickly. When load current is bigger than current-limit threshold value, the output voltage will fall out of the required regulation range. The undervoltage protection circuit continually monitors the FB voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the undervoltage threshold, the under-voltage threshold is 70% of the nominal output voltage, the internal UVP delay counter starts to count. After 16μs debounce time, the device turns off both high-side and low-side MOSEFET with latched and starts a soft-stop process to shut down the output gradually. Toggling enable pin to low or recycling VCC,will clear the latch and bring the chip back to operation.When Short-circuit is't occurs the chip can auto rework.

Over-Voltage Protection (OVP)

The over-voltage function monitors the output voltage by FB pin. When the FB voltage increases over 125% of the reference voltage due to the high-side MOSFET failure or for other reasons, the over-voltage protection comparator designed with a 1.5μs noise filter will force the lowside MOSFET gate driver fully turn on and latch high. This action actively pulls down the output voltage.This OVP scheme only clamps the voltage overshoot and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It's a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can only be reset by toggling EN, VCC power-on-reset signal.The chip will auto rework when Voltage normal.

Current-Limit

The current-limit circuit employs a "valley" current-sensing algorithm (See Figure 2). The TD1730 uses the low-side MOSFET's RDS(ON) of the synchronous rectifier as a current-sensing element. If the magnitude of the current-sense signal at PHASE pin is above the currentlimit threshold, the PWM is not allowed to initiate a new cycle. The actual peak current is greater than the currentlimit threshold by an amount equals to the inductor ripple current. Therefore, the exact current-limit characteristic and maximum load capability are the functions of the sense resistance, inductor value, and input voltage.

Function Description(Cont.)

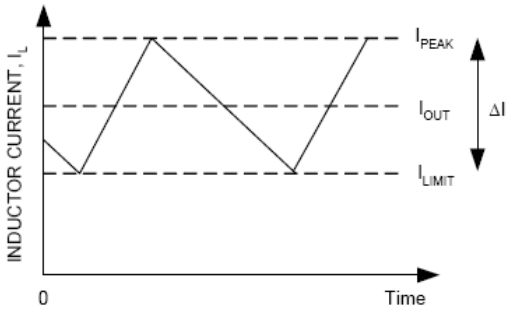


Figure 2. Current-Limit Algorithm

The PWM controller uses the low-side MOSFETs on-resistance RDS(ON) to monitor the current for protection against shortened outputs. The MOSFET's RDS(ON) is varied by temperature and gate to source voltage, the user should determine the maximum RDS(ON) in manufacture's datasheet.

The OCSET pin can source 10μA through an external resistor for adjusting current-limit threshold. The voltage at OCSET pin is equal to 10μA x ROCSET. The relationship between the sampled voltage VOCSET and the current-limit threshold ILIMIT is given by:

$$\frac{1}{8} \times 10\,\mu A \times R_{OCSET} = I_{LIMIT} \times R_{DS(ON)}$$

Where ROCSET is the resistor of current-limit setting threshold. RDS(ON) is the low side MOSFETs conducive resistance. ILIMIT is the setting current-limit threshold. ILIMIT can be expressed as IOUT minus half of peak-to-peak inductor current.

The PCB layout guidelines should ensure that noise and DC errors do not corrupt the current-sense signals at PHASE. Place the hottest power MOSEFTs as close to the IC as possible for best thermal coupling. When combined with the under-voltage protection circuit, this current-limit method is effective in almost every circumstance. The chip will auto rework when Current normal.

Over-Temperature Protection (OTP)

When the junction temperature increases above the rising threshold temperature TOTR, the IC will enter the overtemperature protection state that suspends the PWM,which forces the UGATE and LGATE gate drivers outputlow. The thermal sensor allows the converters to start a start-up process and regulate the output voltage again after the junction temperature cools by 25oC. The OTP is designed with a 25oC hysteresis to lower the average TJ during continuous thermal overload conditions, which increases lifetime of the TD1730. The chip will auto rework when junction temperature normal.

Programming the On-Time Control and PWM Switching Frequency

The TD1730 does not use a clock signal to produce PWM. The device uses the constant-on-time control architecture to produce pseudo-fixed frequency with input voltage feed-forward. The on-time pulse width is proportional to output voltage VOUT and inverses proportional to input voltage VIN. The switching frequency is selectable from four preset values by a resistor connected to RF pin as shown in Table1.

TD1730 doesn't have VIN pin to calculate on-time pulse width. Therefore, monitoring VPHASE voltage as input voltage to calculate on-time when the high-side MOSFET is turned on. And then, use the relationship between ontime and duty cycle to obtain the switching frequency.

Resistance RRF(kΩ)	Switching Frequency Fsw(Khz)
470	135
200	165
100	185
39	215

Application Information

Output Voltage Setting

The output voltage is adjustable from 0.7V to 5.5V with a resistor-divider connected with FB, GND, and converter's output. Using 1% or better resistors for the resistor-divider is recommended. The output voltage is determined by:

$$V_{OUT} = 0.7 \times \left(1 + \frac{R_{TOP}}{R_{GND}}\right)$$

Where 0.7 is the reference voltage, RTOP is the resistor connected from converter's output to FB, and RGND is the resistor connected from FB to GND. Suggested RGND is in the range from 1k to 20kΩ. To prevent stray pickup, locate resistors RTOP and RGND close to TD1730.

Output Inductor Selection

The duty cycle (D) of a buck converter is the function of the input voltage and output voltage. Once an output voltage is fixed, it can be written as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

The inductor value (L) determines the inductor ripple current, IRIPPLE, and affects the load transient reponse. Higher inductor value reduces the inductor's ripple current and induces lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

Where FSW is the switching frequency of the regulator.Although the inductor value and frequency are increased and the ripple current and voltage are reduced, a tradeoff exists between the inductor's ripple current and the regulatorload transient response time.

A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current. Increasing the switching frequency (FSW) also reduces the ripple current and voltage, but it will increase the switching loss of the MOSFETs and the power dissipation of the converter. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current. Once the inductance value has been chosen, selecting an inductor which is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is made of ferrite, the ripple current will increase abruptly when it saturates. This results in a larger output ripple voltage. Besides, the inductor needs to have low DCR to reduce the loss of efficiency.

Output Capacitor Selection

Output voltage ripple and the transient voltage deviation are factors which have to be taken into consideration when selecting an output capacitor. Higher capacitor value and lower ESR reduce the output ripple and the load transient drop. Therefore, selecting high performance low ESR capacitors is recommended for switching regulator applications. In addition to high frequency noise related to MOSFET turn-on and turnoff,the output voltage ripple includes the capacitance voltage drop ΔVCOUT and ESR voltage drop ΔVESR caused by the AC peak-to-peak inductor's current. These two voltages can be represented by:

$$\Delta V_{COUT} = \frac{I_{RIPPLE}}{8 C_{OUT} F_{SW}}$$

$$\Delta V_{ESR} = I_{RIPPLE} \times R_{ESR}$$

These two components constitute a large portion of the total output voltage ripple. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If the output of the converter has to support another load with high pulsating current, more capacitors are needed in order to reduce the equivalent ESR and suppress the voltage ripple to a tolerable level. A small decoupling capacitor (1μF) in parallel for bypassing the noise is also recommended, and the voltage rating of the output capacitors are also must be considered.To support a load transient that is faster than the switching frequency, more capacitors are needed for reducing the voltage excursion during load step change. Another aspect of the capacitor selection is that the total AC current going through the capacitors has to be less than the rated RMS current specified on the capacitors in order to prevent the capacitor from over-heating.

Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, selecting the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately IOUT/2,where IOUT is the load current. During power-up, the input capacitors have to handle great amount of surge current.For low-duty notebook appliactions, ceramic capacitor is recommended. The

Application Information(Cont.)

capacitors must be connected between the drain of high-side MOSFET and the source of low-side MOSFET with very low-impeadance PCB layout.

MOSFET Selection

The application for a notebook battery with a maximum voltage of 24V, at least a minimum 30V MOSFETs should be used. The design has to trade off the gate charge with the RDS(ON) of the MOSFET:

For the low-side MOSFET, before it is turned on, the body diode has been conducting. The low-side MOSFET driver will not charge the miller capacitor of this MOSFET.In the turning off process of the low-side MOSFET, the load current will shift to the body diode first. The high dv/dt of the phase node voltage will charge the miller capacitor through the low-side MOSFET driver sinking current path. This results in much less switching loss of the lowside MOSFETs. The duty cycle is often very small in high battery voltage applications, and the low-side MOSFET will conduct most of the switching cycle; therefore, when using smaller RDS(ON) of the low-side MOSFET, the converter can reduce power loss. The gate charge for this MOSFET is usually the secondary consideration.

The high-side MOSFET does not have this zero voltage switching condition; in addition, because it conducts for less time compared to the low-side MOSFET, the switching loss tends to be dominant. Priority should be given to the MOSFETs with less gate charge, so that both the gatedriver loss and switching loss will be minimized.

The selection of the N-channel power MOSFETs are determined by the $R_{DS(ON)}$, reversing transfer capacitance (C_{RSS}) and maximum output current requirement.

The losses in the MOSFETs have two components:conduction loss and transition loss. For the high-side and low-side MOSFETs, the losses are approximately given by the following equations:

$$P_{high\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})D + (0.5)(I_{OUT})(V_{IN})(t_{SW})F_{SW}$$
$$P_{low\text{-}side} = I_{OUT}^{2}(1+TC)(R_{DS(ON)})(1-D)$$

Where

IOUT is the load current

TC is the temperature dependency of RDS(ON)

FSW is the switching frequency

tSW is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the high-side MOSFET includes an additional transition loss.The switching interval, tSW, is the function of the reverse transfer capacitance CRSS. The (1+TC) term is a factor in the temperature dependency of the RDS(ON) and can be extracted from the “RDS(ON) vs. Temperature” curve of the power MOSFET.

Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator.With power devices switching at higher frequency, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off condition, the MOSFET is carrying the full load current. During turn-off,current stops flowing in the MOSFET and is freewheeling by the low side MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. Besides, signal and power grounds are to be kept separating and finally combined using ground plane construction or single point grounding. The best tie-point between the signal ground and the power ground is at the negative side of the output capacitor on each channel, where there is less noise. Noisy traces beneath the IC are not recommended. Below is a checklist for your layout:

·Keep the switching nodes (UGATE, LGATE, BOOT,and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals.Therefore, keep traces to these nodes as short as possible and there should be no other weak signal traces in parallel with theses traces on any layer.

·The signals going through theses traces have both high dv/dt and high di/dt with high peak charging and discharging current. The traces from the gate drivers to the MOSFETs (UGATE and LGATE) should be short and wide.

·Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible.Minimizing the impedance with wide

Application Information(Cont.)

layout plane between the two pads reduces the voltage bounce of the node. In addition, the large layout plane between the drain of the MOSFETs (VIN and PHASE nodes) can get better heat sinking.

·The GND is the current sensing circuit reference ground and also the power ground of the LGATE lowside MOSFET. On the other hand, the GND trace should be a separate trace and independently go to the source of the low-side MOSFET. Besides, the current sense resistor should be close to OCSET pin to avoid parasitic capacitor effect and noise coupling.

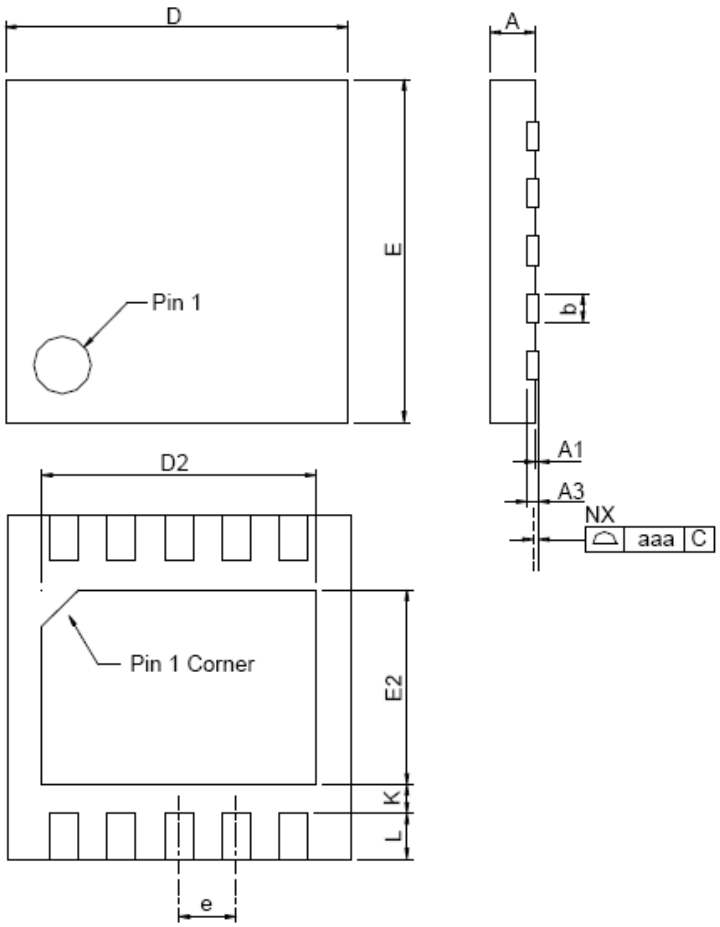
·Decoupling capacitors, the resistor-divider, and boot capacitor should be close to their pins. (For example,place the decoupling ceramic capacitor close to the drain of the high-side MOSFET as close as possible.)

·The input bulk capacitors should be close to the drain of the high-side MOSFET, and the output bulk capacitors should be close to the loads. The input capacitor's ground should be close to the grounds of the output capacitors and low-side MOSFET.

·Locate the resistor-divider close to the FB pin to minimize the high impedance trace. In addition, FB pin traces can't be close to the switching signal traces(UGATE, LGATE, BOOT, and PHASE).

Package Information

TDFN3x3-10



SYMBOL	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Design Notes