Alpha Microelectronics Corp.

AM5AA OTP Series II (085x/171x) DATA SHEET

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Revision History

Rev	Date	Description	Page
1.00	2016/2/16	New Release	-

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Table of Contents

1 General Description

AM5AA OTP Series II (085x/171x) (Henceforth **"AM5AA OTP Series II"**) is a 4-bit microprocessor with the advantages of low cost and high voice quality. There are various features in AM5AA OTP Series II, including 4-bit ALU, ROM, RAM, I/O ports, timers, interrupt, clock generator and PWM outputs, etc. Among these, functions such as Watchdog Timer (WDT), Low Voltage Reset (LVR), and Infrared Ray Transmitter (IR) will reduce the system cost and enhance reliability. In addition, large current outputs significantly diversify AM5AA OTP Series II applications; meanwhile, with CMOS technology, SLEEP function can minimize power dissipation. RISC MCU architecture is very easy to program and control. There is a total of 31 instructions in AM5AA OTP Series II, most of which are executed only in a single cycle. In the output stage, user can select the direct-drive (PWM) to output the audio data or configure the two audio pins as PWMIO.

2 Features

(1) Single power supply can operate from 1.8 V to 5.5 V at 8 MHz and 2.0 V to 5.5 V at 12 MHz for AM5AA OTP Series II.

(2) Program ROM can be up to 64k x 10-bit (0000H ~ FFFFH).

(3) Rom size and key features:

Product	Voice Duration (sec)	ROM Size (10-bit)	Clock Source	Audio Output	Volume Control	IR	Reset
AM5AA085x	84	224k	RM	PWM	v	PRA[2]	PRA[3]
AM5AA171x	170	448k	RM	PWM	v	PRA[2]	PRA[3]

(4) The symbol "v" in the following table means that AM5AX series can be tested and verified by AM5AA OTP Series II, but it is not guaranteed to be workable in the opposite way.

AM5AX / AM5AA	AM5AB Series	AM5AC Series	AM5AD Series	AM5AE Series
AM5AA085x	v*	v	x	x
AM5AA171x	v*	v*	v	x

*: If the I/O pin numbers of AM5AX series and AM5AA OTP Series II are different, the unused I/O pin must be set as output in case any unexpected error occurs.

(5) I/O Ports

Product	I/O Pins	Port Name
AM5AA085x	8	PRA ~ PRB
AM5AA171x	12	PRA ~ PRC

(6) Each pin of all ports can be a wake-up port when configured as an input.

(7) Support at most 4-level Stack, which can be used as data SRAM for additional 16 x 4-bit space.

Product	Data SRAM	4-Level Stack or Used As Additional Data SRAM
AM5AA085x	120 x 4 (18H ~ 8FH)	16 x 4 (90H ~ 9FH)
AM5AA171x		

(8) Sleep Mode

System clock is totally stopped when entering Sleep Mode, in which all functions will stop to save power. User can wake up AM5AA OTP Series II from Sleep Mode by changing data of the input port.

(9) Each I/O pin can be controlled by three I/O registers:

a) I/O direction register

b) I/O data register

c) I/O pull-low register

(10) There are two ports with large current outputs: PRA[0] ~ PRA[3] and PRB[0] ~ PRB[3] for AM5AA085x, as well as PRA[0] ~ PRA[3] and PRB[0] ~ PRB[3] and PRC[0] ~ PRC[3] for AM5AA171x

(11) Low-cost OSC: **(Code Option)**

PRA[0] can be selected as a general I/O or an OSC pin.

(12) Built-in Infrared Ray (IR) carrier output: **(Code Option)**

There is a built-in IR carrier output pin in AM5AA OTP Series II which can be used as a transmission pin for wireless transmission. User can set PRA[2] as the IR carrier pin. Through code option, the built-in IR carrier output can be switched to high or low, and the frequency can be set as 38K or 56K.

(13) AM5AA OTP Series II contains one voice channel and only supports software decoder for the voice channel.

(14) Audio output method:

The 10-bit direct-drive output (PWM) is supported to provide best audio output quality.

(15) 8-level volume control. **(Register Control)**

(16) 4-level stack SRAM space is shared by the interrupt. There is only one interrupt source, that is SR timer overflowing.

(17) There are 4 kinds of reset:

a) Power-on reset

b) Watchdog Timer reset

c) Low voltage reset

d) External reset

(18) External reset: User can set PRA[3] as a reset pin. **(Code Option)**

(19) Number of instructions: 31.

(20) PWMIO function is supported. **(Code Option)**

The audio pins PWM1 and PWM2 are not only audio output pins, but also data output pins.

Note: In Sleep Mode, both PWM1 and PWM2 are floating.

3 Memory Organization

3.1 ROM

ROM memory is divided into five portions. The first portion 0x0~0xF is the address range for the reset vector in the normal mode. The second portion 0x10~0x1F is the address range for the interrupt vector in the normal mode. The third portion 0x20~0x1FF is reserved and not available for storing programs. The fourth portion 0x200~0xFFFF is the address range for user main program and voice data. The last portion 0x10000~0xXFFFF could be used to store the voice data. For AM5AA OTP Series II, JMP and CALL instructions can only reach an immediate address within a 16-bit wide page, the main program and ISR therefore can only be located in the 0x200~0xFFFF address range. In addition, except for Program Counter (PC), all pointers such as voice pointer (VPTR) and temporary register (TREG) can reach up to 0xXFFFF. FIGURE 3.1 shows the ROM map.

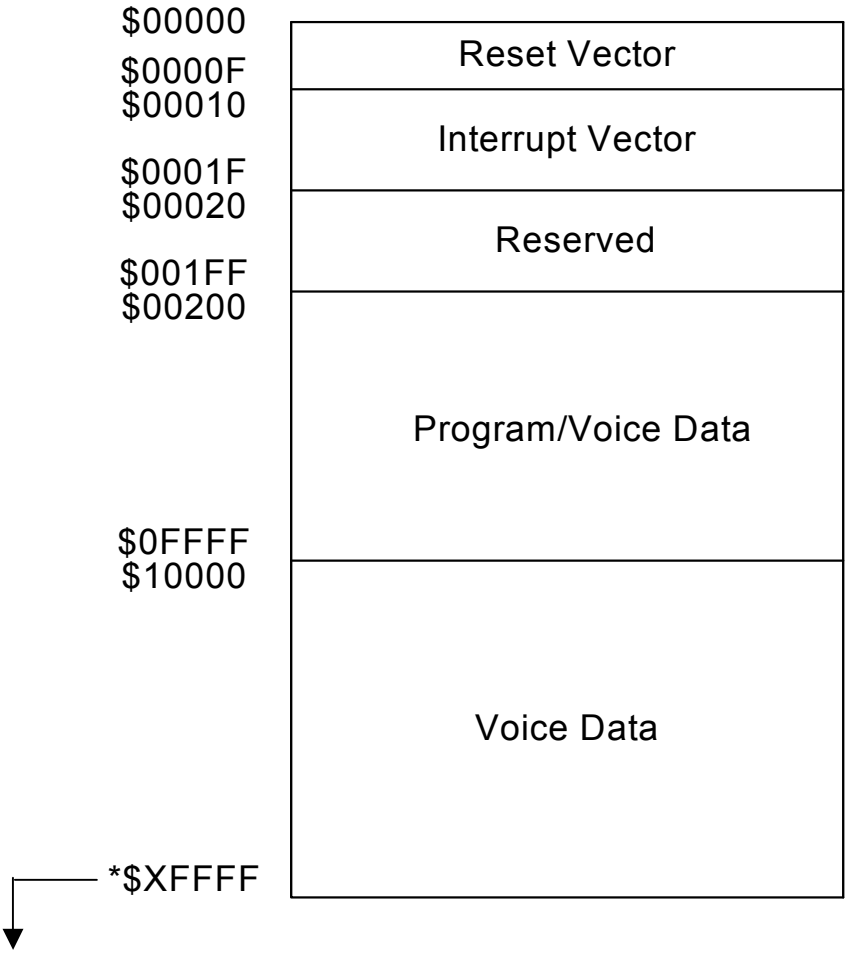


FIGURE 3.1 ROM Map of AM5AA_OTP

AM5AA085x is $37FFF

AM5AA171x is $6FFFF

3.2 SRAM

SRAM is composed of special function register (SFR), working SRAM, general SRAM and stack SRAM. Address 0x00~0x17 is reserved for SFR. Address 0x18~0x2F is for the working SRAM which can be executed with logic or arithmetic instructions. Address 0x30~0x8F is for the general SRAM and address 0x90~0x9F is for the stack SRAM. The stack SRAM is reserved for storing the current PC value when a CALL instruction or interrupt occurs.

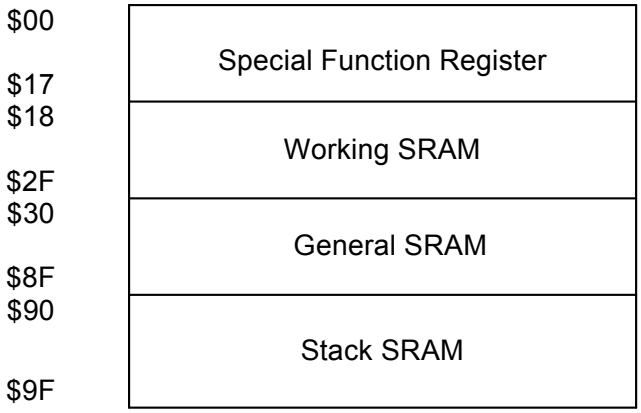


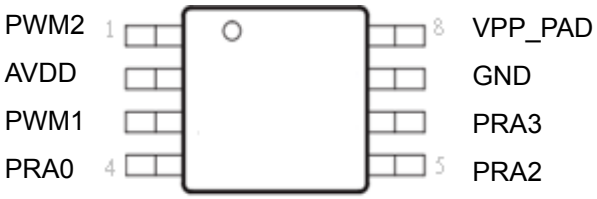
FIGURE 3.2 SRAM Map of AM5AA_OTP

4 Pin Configuration and Pin Description

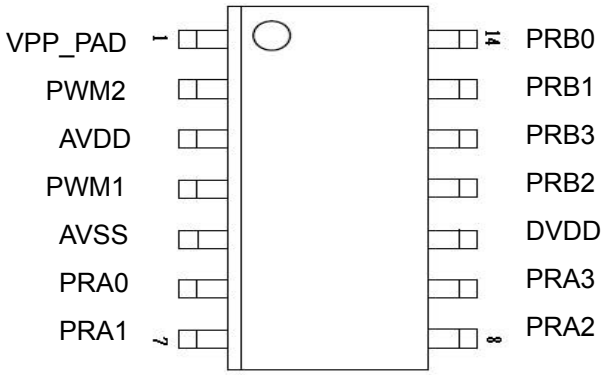
4.1 Pin Configuration

4.1.1 AM5AA085x

4.1.1.1 8 Pin – AM5AA085AW/AX (PDIP/SOP)

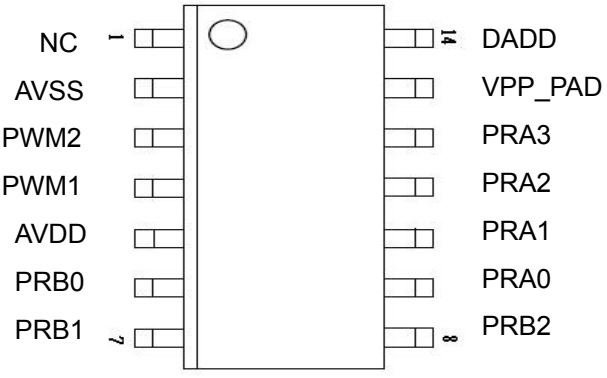


4.1.1.2 14 Pin – AM5AA085AP/AS (PDIP/SOP)

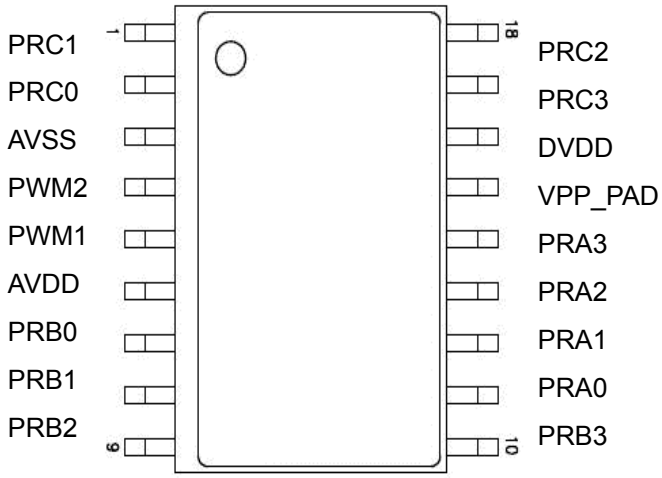


4.1.2 AM5AA171x

4.1.2.1 14 Pin – AM5AA171AW/AX (PDIP/SOP)



4.1.2.2 18 Pin – AM5AA171AP/AS (PDIP/SOP)



4.2 Pin Description

Pin Name	Attr.	Description
PRA[0]	I/O	This I/O pin can be programmed to input / output individually. Input type with weak pull-low or input-floating capability. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an OSC pin. **(Code Option)**
PRA[2] **/ IR**	I/O	This I/O pin can be programmed to input / output individually. Input type with weak pull-low or input-floating capability. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an IR Carrier Output pin with programmable 37 KHz. **(Code Option)**
PRA[3] **/ Reset**	I/O	This I/O pin can be programmed to input / output individually. Input type with weak pull-low or input-floating capability. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)** Or selected as an external RESET pin with weak pull-low capability. **(Code Option)**
PRA[1] **PRB[0]~PRB[3]** **PRC[0]~PRC[3]**	I/O	This I/O pin can be programmed to input / output individually. Input type with weak pull-low or input-floating capability. Buffer Output type. Or 2 kinds of output current: (1) Normal current, (2) Large current. **(Code Option)**
PWM1	O	PWM1 output
PWM2	O	PWM2 output.
AVDD	Power	Positive power supply for analog portion.
DVDD	Power	Positive power supply for digital portion.
AVSS/DVSS	Power	Ground Potential.
VPP_PAD	Power	Leave it NC (not connected) during normal operation. Connect to a high voltage when programming EPROM.

5 Electrical Characteristics

The electrical characteristics of AM5AA OTP Series II series are given in the following tables in which all the data are measured at room temperature. Various production processes among lots or different testing conditions may influence the data result.

5.1 Absolute Maximum Rating

SYMBOL	RATING	UNIT
V_{SS} ~ V_{DD}	-0.5 ~ +6.0	V
V_{in} (All input)	V_{SS}-0.3 < V_{in} < V_{DD}+0.3	V
V_{out} (All output)	GND < V_{out} < V_{DD}	V
T_{OP} (Operating)	0 ~ +70	℃
T_{ST} (Storage)	-25 ~ +85	℃

5.2 DC Characteristics

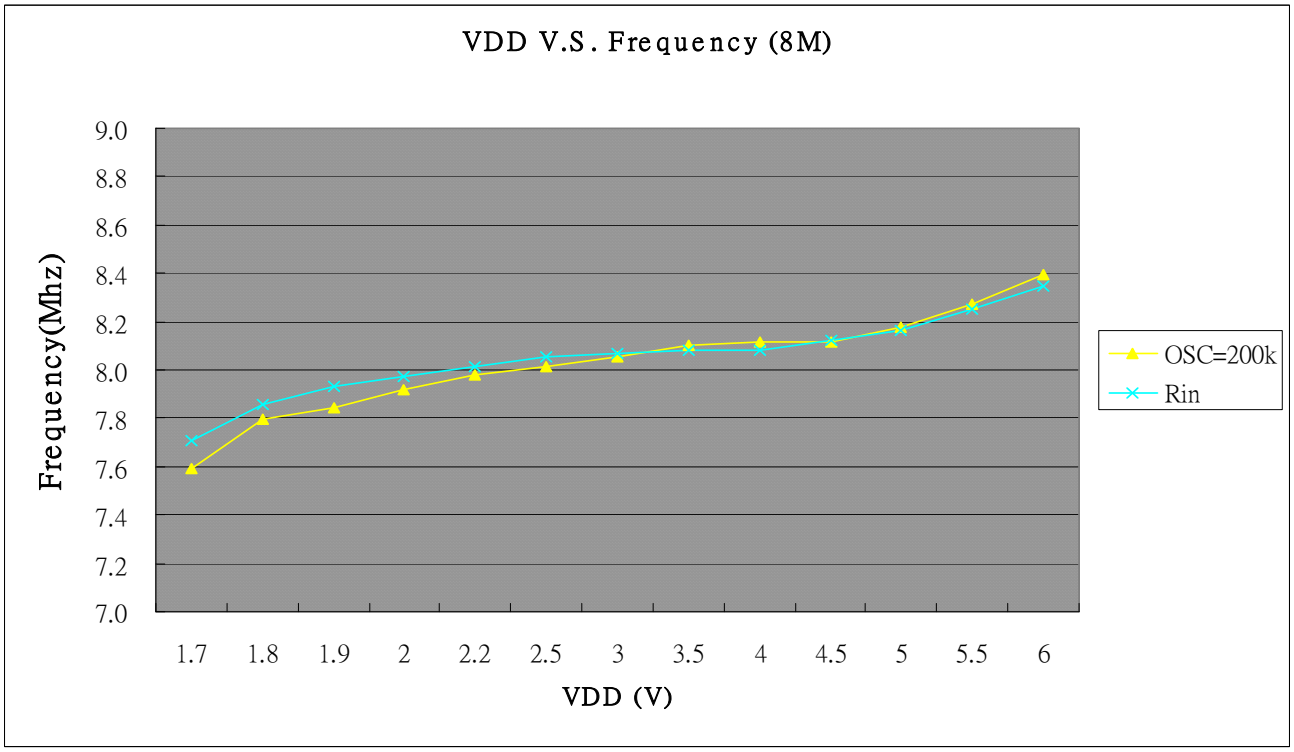
SYMBOL	PARAMETER		V_{DD}	MIN.	TYP.	MAX.	UNIT	CONDITION
V_{DD}	Operating Voltage			1.8	3	5.5	V	8 MHz
				2.0	3	5.5		12 MHz
LVR	Low Voltage Reset				1.8±0.1		V	8 MHz
					2.0±0.1			12 MHz
I_{ht}	Supply Current	Sleep	3			1	uA	Sleep Mode
			4.5			2		
I_{OP}		Operating	3		3.3		mA	8 MHz, RM, I/O No Loads
			4.5		4.3			
			3		3.4			12 MHz, RM, I/O No Loads
			4.5		4.4			
I_{IH}	Input Current (Internal weak pull-low)		3		-2.96		uA	V_{IL} = 0 V
			4.5		-8.89			
I_{OH}	Output High Current (Normal current)		3		-5.13		mA	V_{OH} = 2.6 V
			4.5		-12.99			V_{OH} = 3.7 V
I_{OH}	eOutput High Currnt (Large current)		3		-6.93			V_{OH} = 2.6 V
			4.5		-17.097			V_{OH} = 3.7 V

SYMBOL	PARAMETER	V_{DD}	MIN.	TYP.	MAX.	UNIT	CONDITION
I_{OL}	Output Low Current (Normal current)	3		7.4			V_{OL} = 0.4 V
		4.5		16.247			V_{OL} = 0.8 V
I_{OL}	Output Low Current (Large current)	3		17.01			V_{OL} = 0.4 V
		4.5		37.417			V_{OL} = 0.8 V
I_{PWM}	PWM Output Current (peak)	3	100			mA	Load = 8 ohms
dF/F	Frequency Stability	3.4		± 3		%	$\frac{Fosc\ (3.4\ V) - Fosc\ (2.2\ V)}{Fosc\ (3.4\ V)}$
dF/F	Frequency Stability	5.1		± 3		%	$\frac{Fosc\ (5.1\ V) - Fosc\ (2.7\ V)}{Fosc\ (5.1\ V)}$
dF/F	F_{OSC} Variation	3	7.76	8	8.24	MHz	8M ± 3%
		4.5					
		3	11.64	12	12.36		12M ± 3%
		4.5					

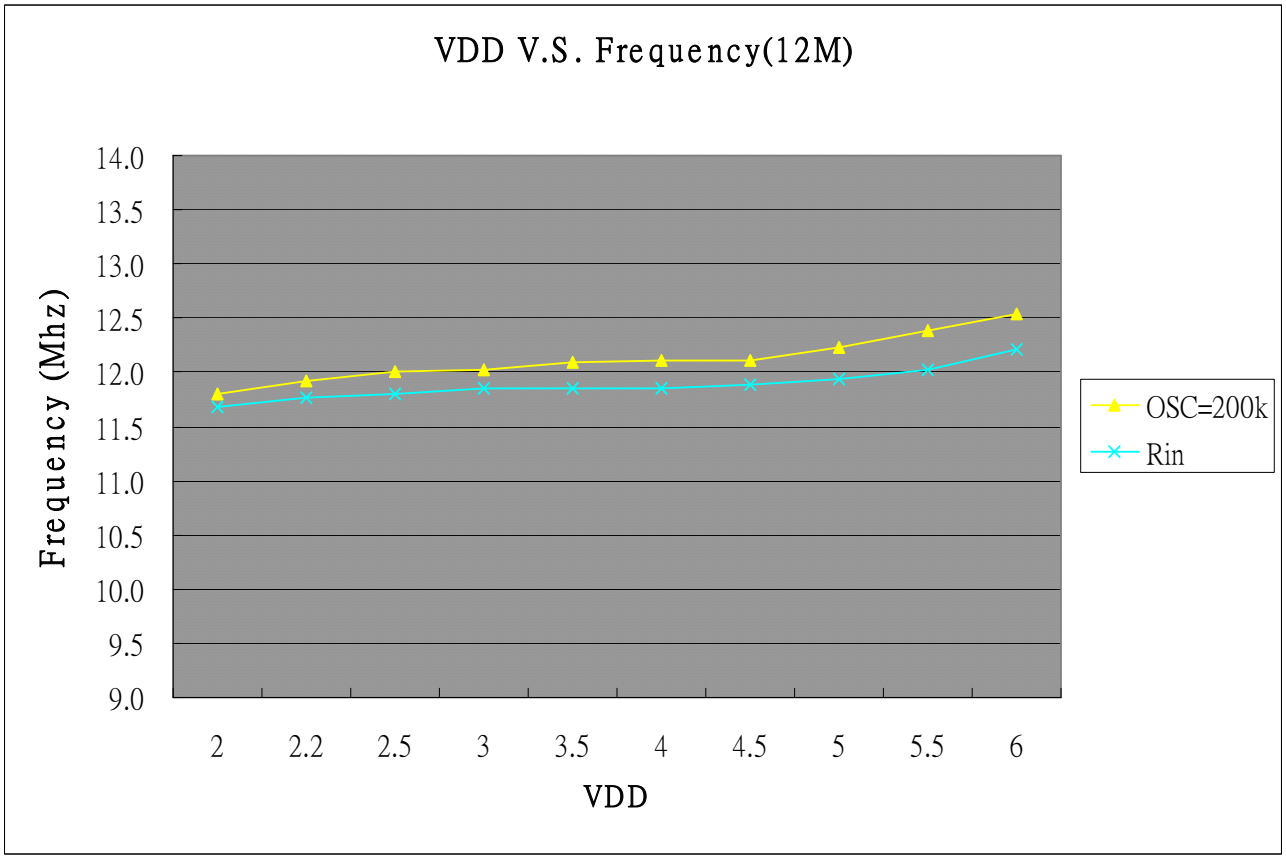
Note: Ambient temperature is 25℃. Alpha will keep user updated when the temperature setting is changed.

5.3 Typical R_{OSC} vs. V_{DD} for RM Mode Oscillator

(1) Using 8 MHz System Clock

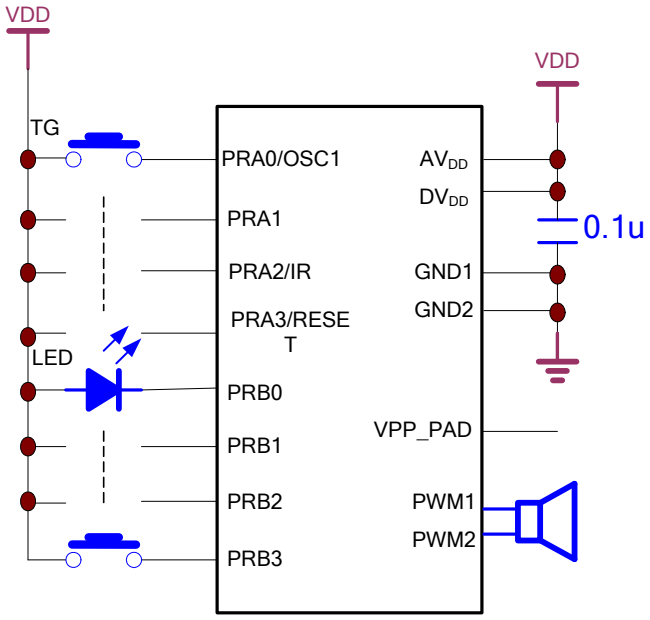


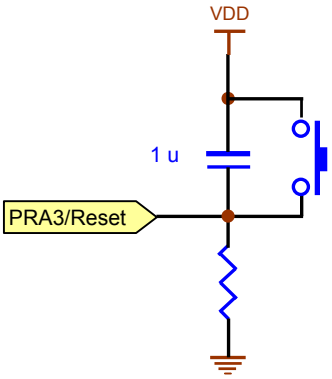
(2) Using 12 MHz System Clock



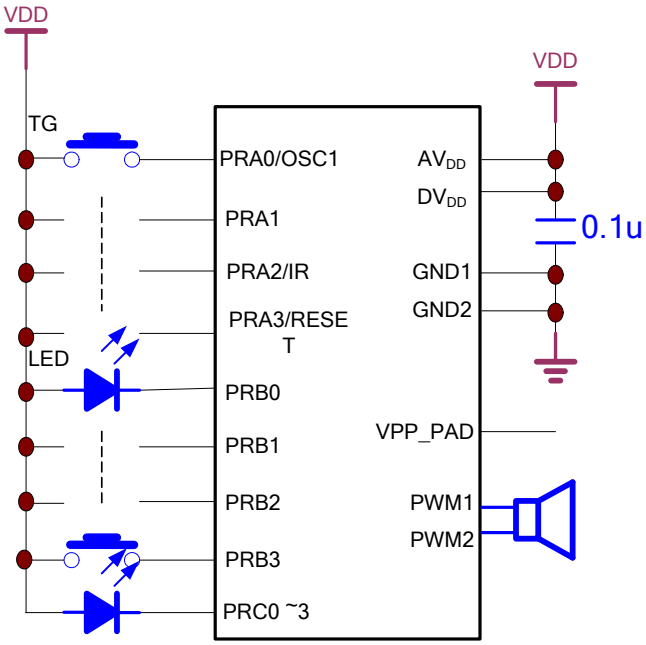
6 Application Circuit

6.1 PRA0 as General I/O Pin





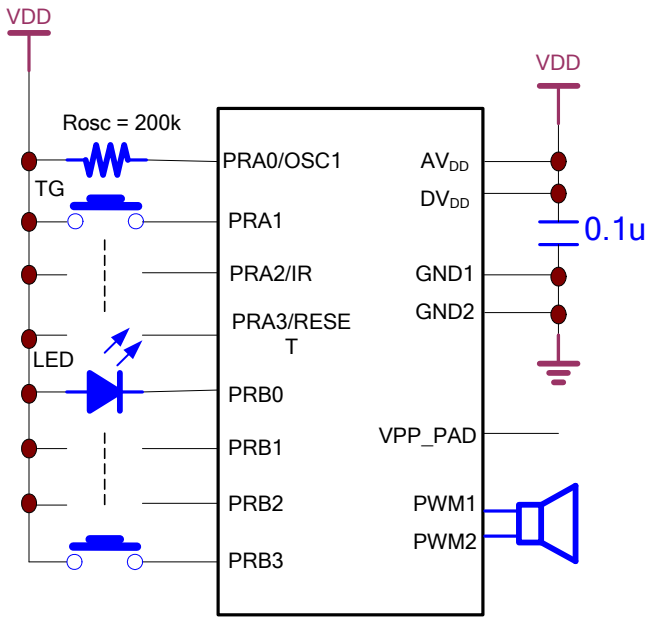
AM5AA085x

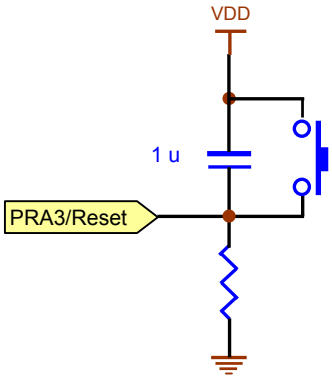


AM5AA171x

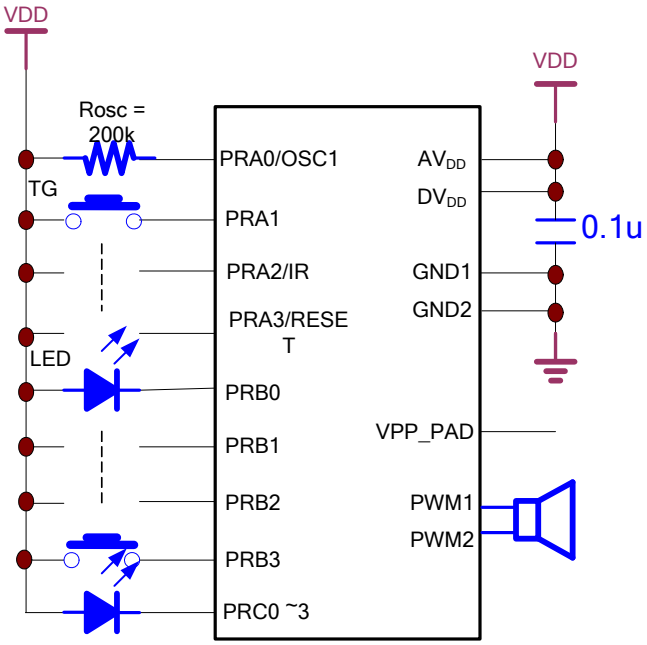
6.2 PRA0 as OSC Pin

6.2.1 External R



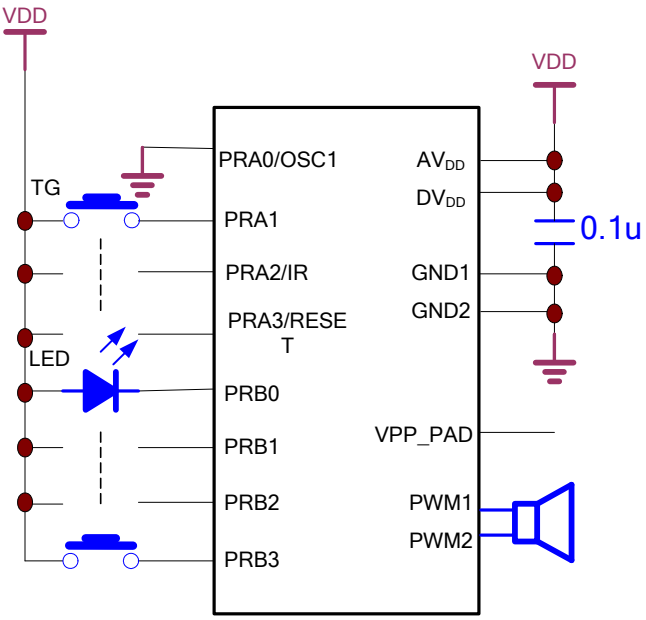


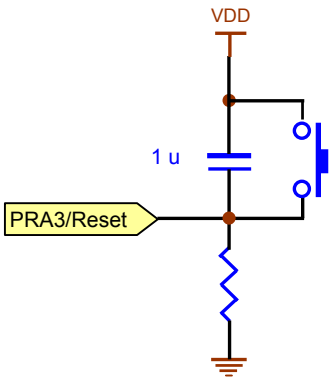
AM5AA085x



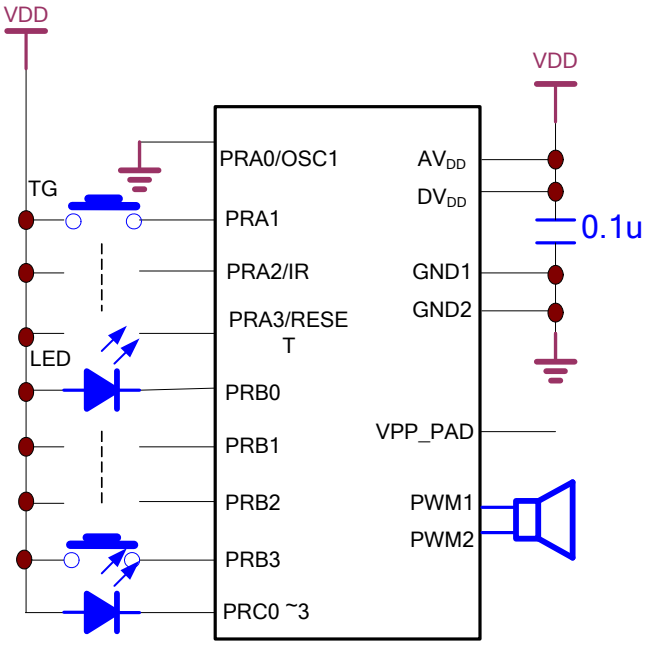
AM5AA171x

6.2.2 Internal R





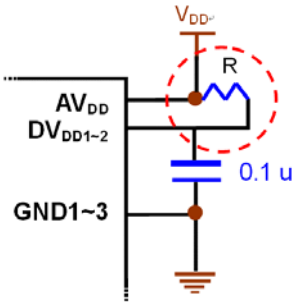
AM5AA085x



AM5AA171x

Note:

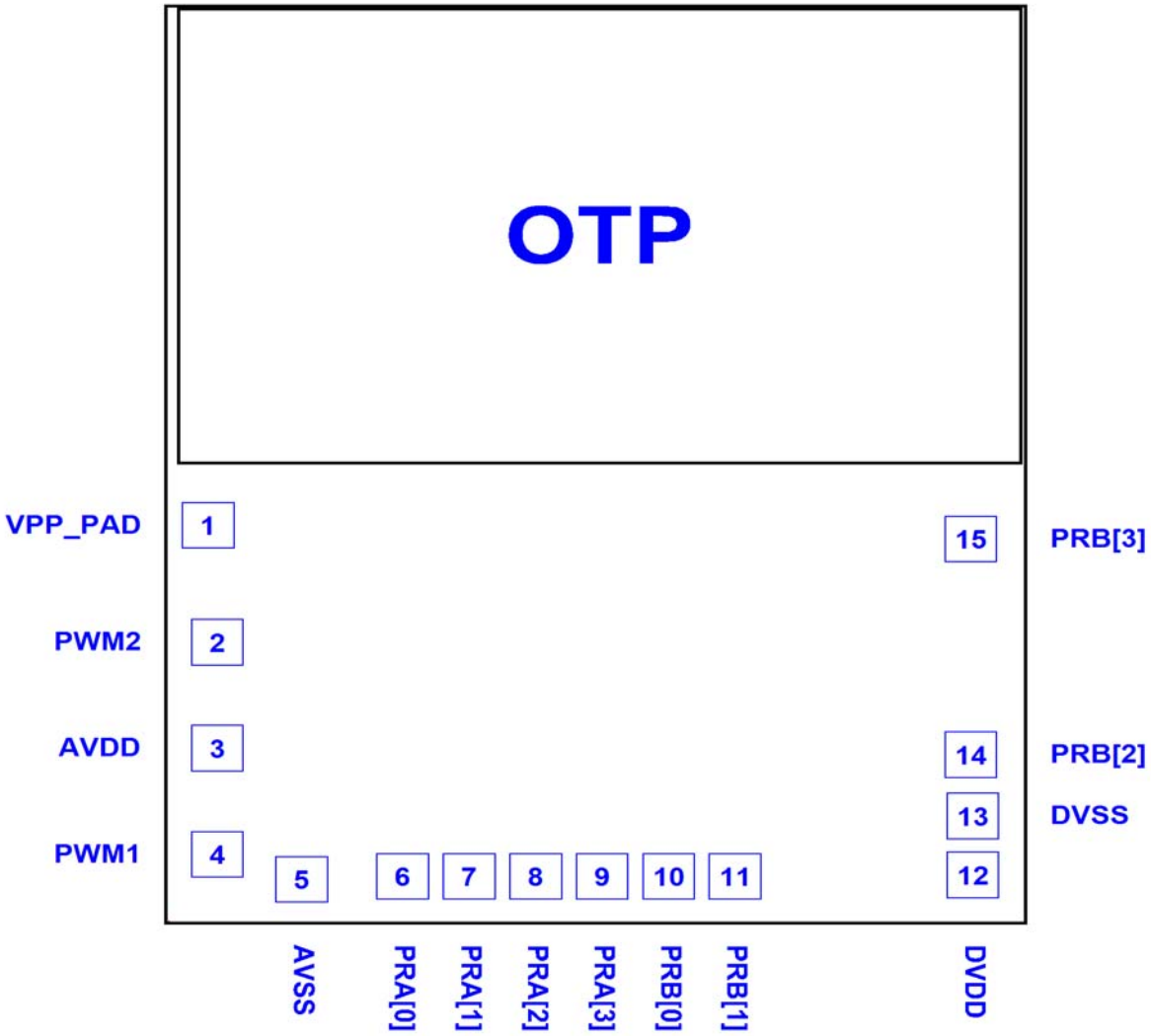
(1) Normally, AV_{DD} and DV_{DD} on both applications should be directly connected to VDD as shown in the above figures. However, in the case of selecting system clock as 12 MHz and working voltage as 3 V, for more stable circuit characteristics, a 10 ohm resistor (R) should be added. The resistor connection is marked in the dashed circle as shown in the figure on the right.



(2) Normally, VPP_PAD should be directly connected to Gnd or floating as shown in the above figures.

7 Pad Location

7.1 AM5AA085x

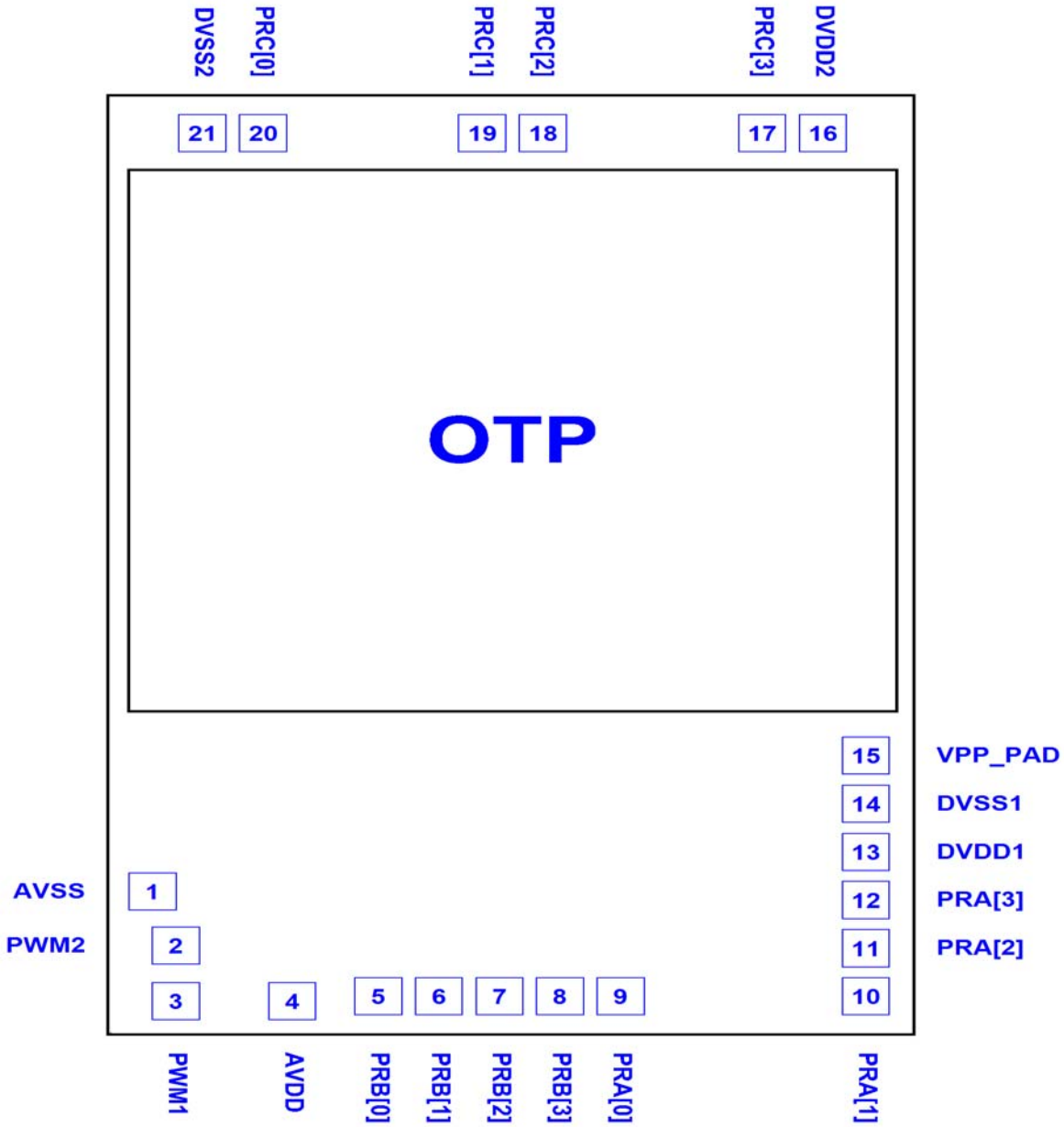


Note:

(1)The IC substrate must be connected to GND.

(2)The VPP_PAD pin must be connected to Gnd or floating if not used.

7.2 AM5AA171x



Note:

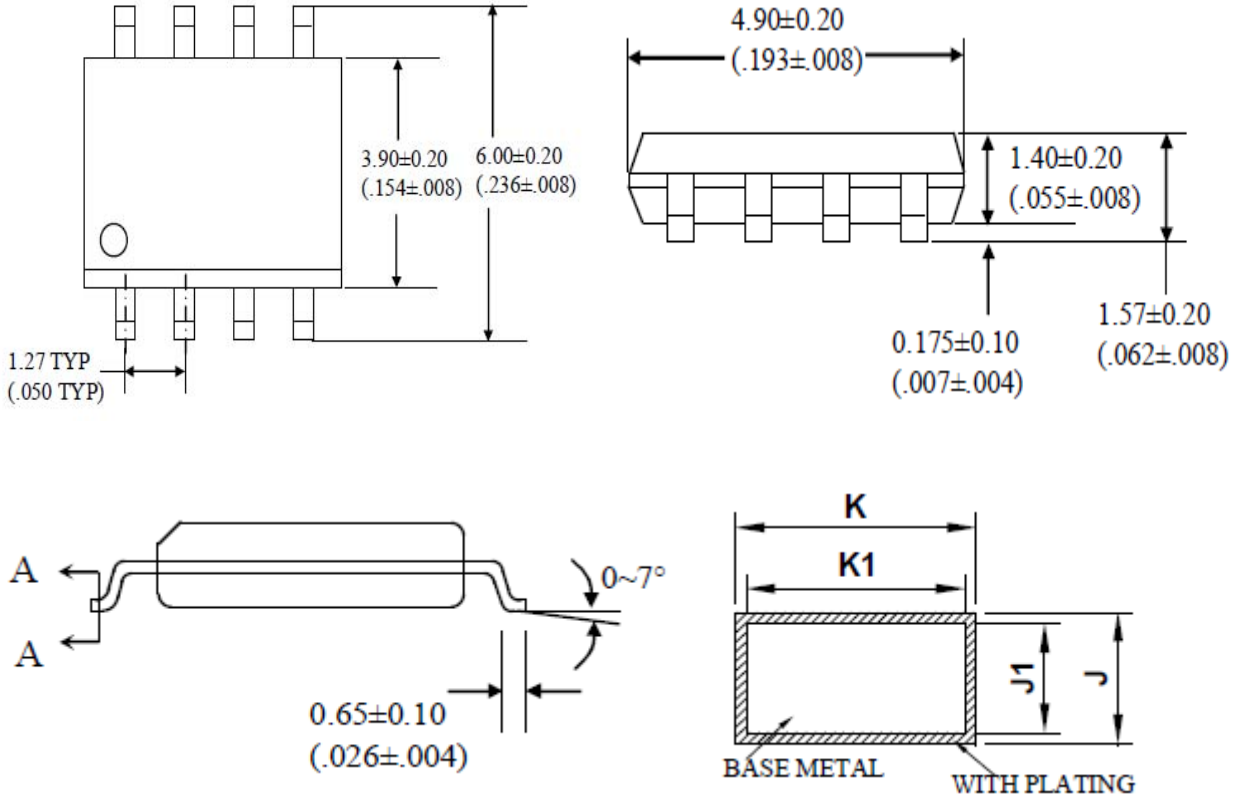
(1) The IC substrate must be connected to GND.

(2) The VPP_PAD pin must be connected to Gnd or floating if not used.

8 Package Dimension

8.1 SOP8L

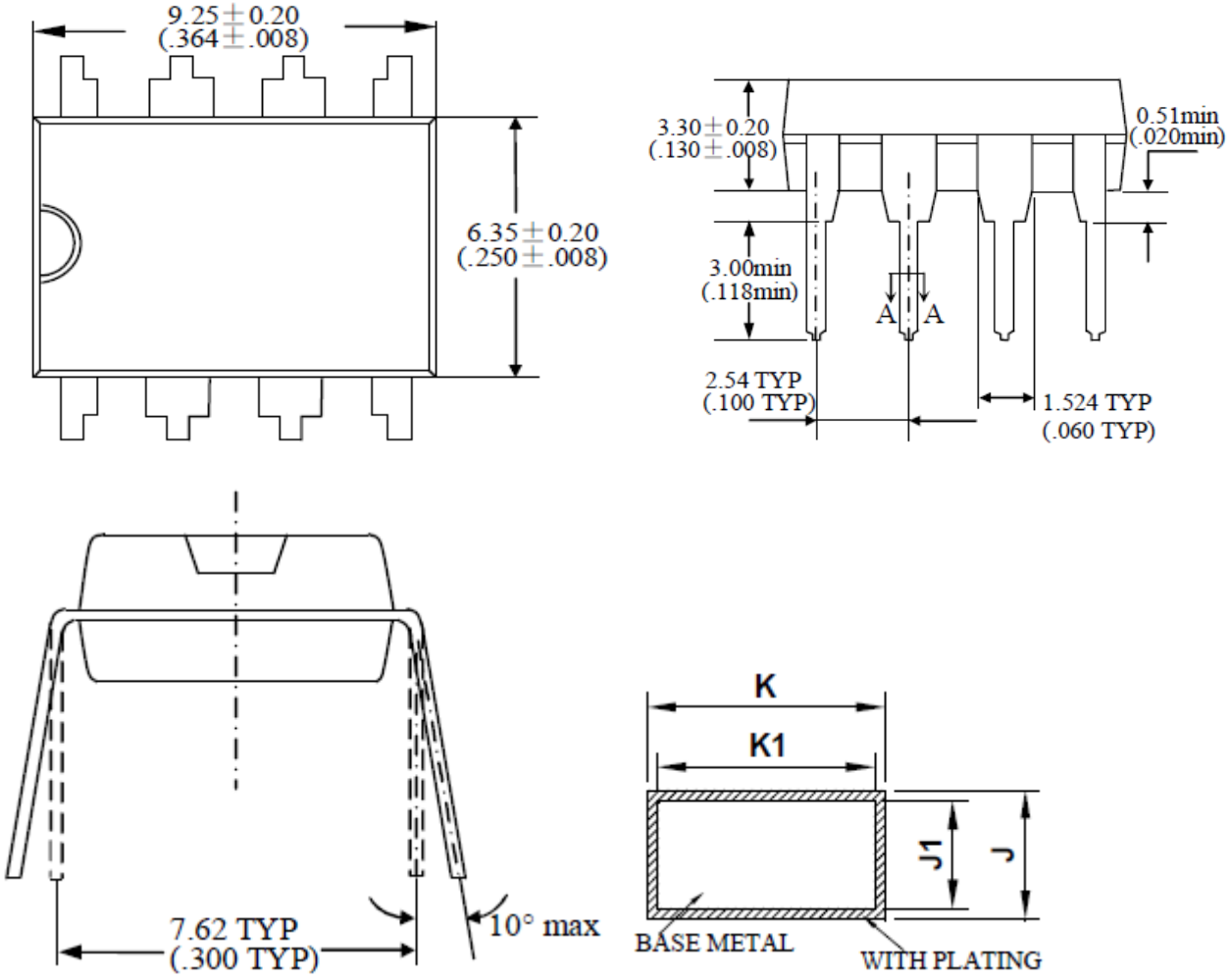
DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
J	0.178	0.278	.0070	.0109
J1	0.178	0.228	.0070	.0090
K	0.406	0.496	.0160	.0195
K1	0.406	0.496	.0160	.0180



Unit : mm (inch)

8.2 PDIP8L

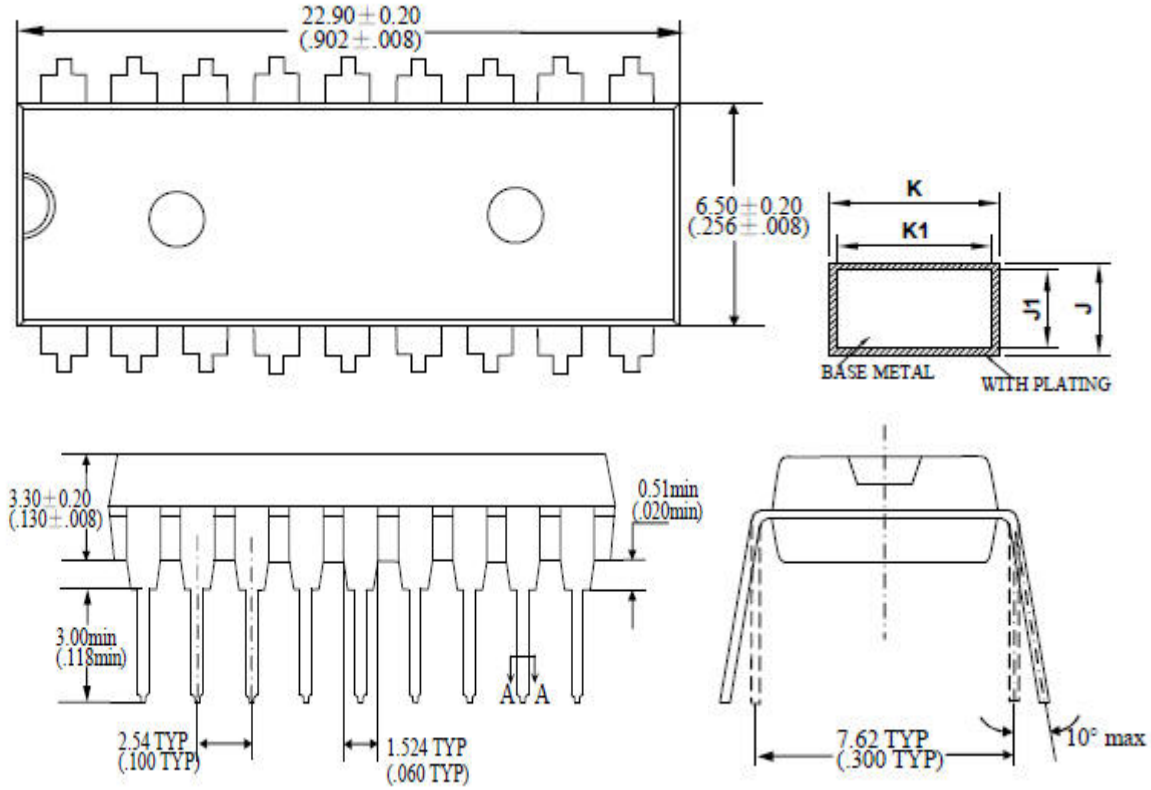
DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
J	0.219	0.339	.0086	.0133
J1	0.219	0.289	.0086	.0114
K	0.460	0.560	.0181	.0220
K1	0.460	0.510	.0181	.0201



Unit : mm (inch)

8.3 SOP14L

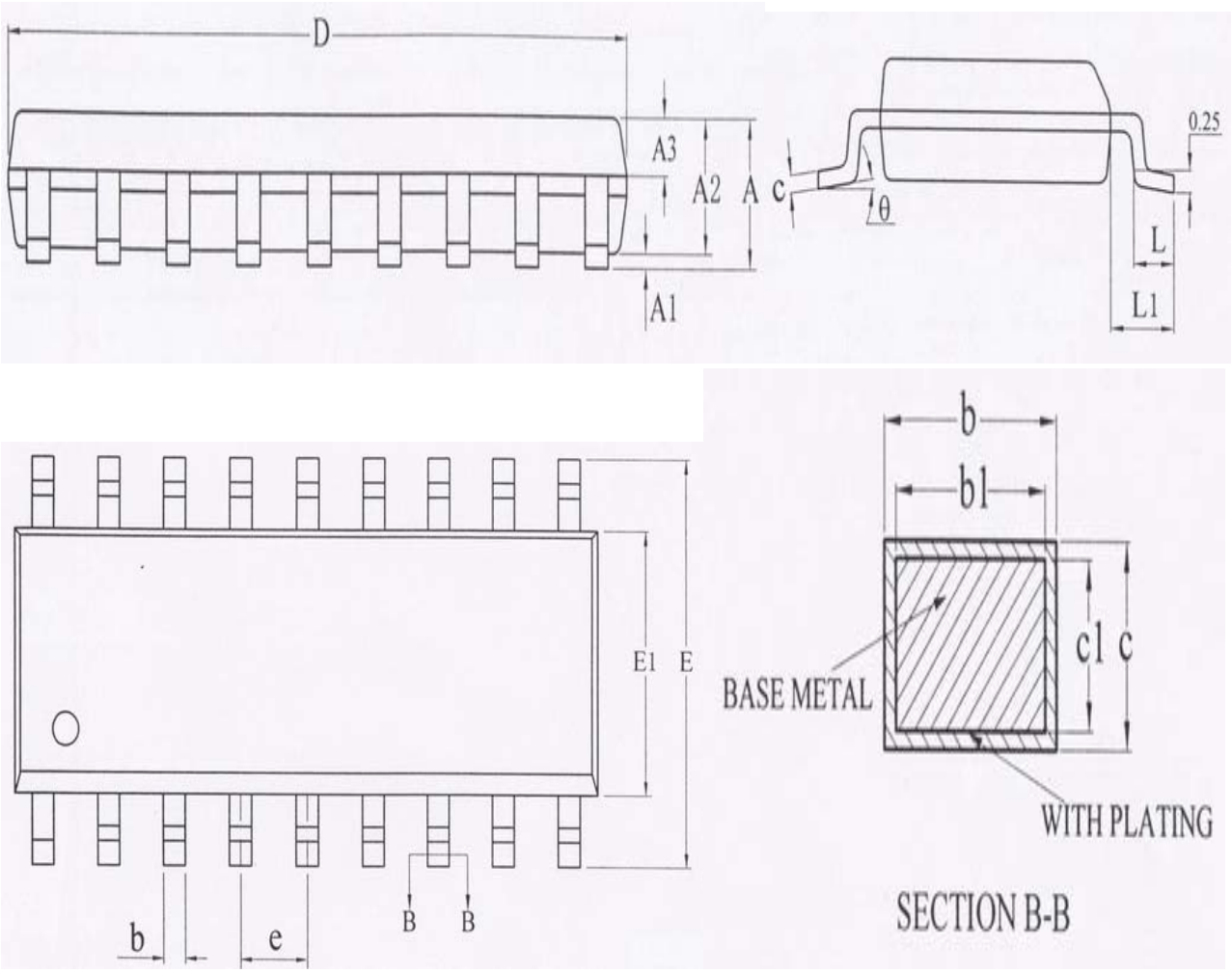
DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
J	0.219	0.339	.0086	.0133
J1	0.219	0.289	.0086	.0114
K	0.460	0.560	.0181	.0220
K1	0.460	0.510	.0181	.0201



Unit : mm (inch)

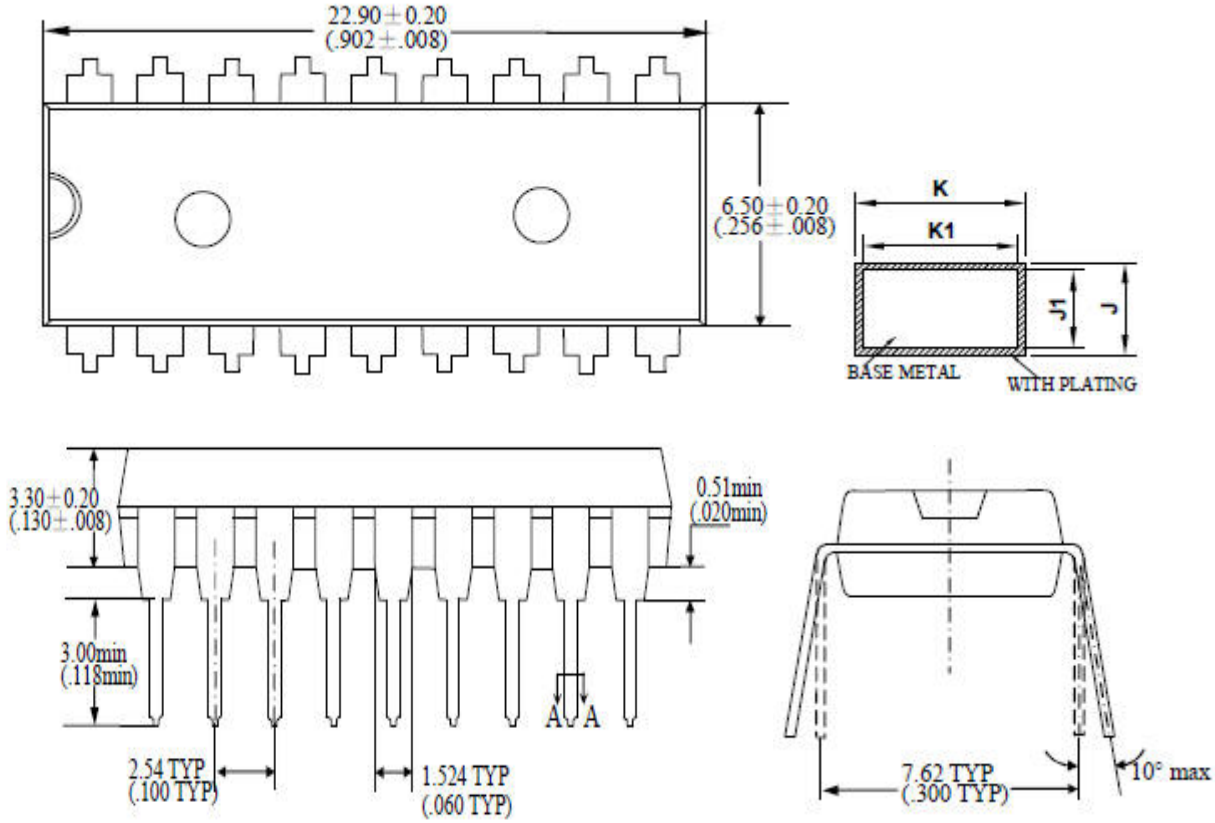
8.4 SOP18L

DIM	MILLIMETERS			DIM	MILLIMETERS		
	MIN.	NOM	MAX.		MIN.	NOM	MAX.
A	—	—	2.70	D	11.25	11.45	11.65
A1	0.08	0.18	0.28	E	10.10	10.30	10.50
A2	2.10	2.30	2.50	E1	7.30	7.50	7.70
A3	0.92	1.02	1.12	e	1.27BSC		
b	0.35	—	0.44	L	0.70	0.85	1.00
b1	0.34	0.37	0.39	L1	1.40BSC		
c	0.26	—	0.31	θ°	0°	—	8°
c1	0.24	0.25	0.26				



8.5 PDIP18L

DIM	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
J	0.219	0.339	.0086	.0133
J1	0.219	0.289	.0086	.0114
K	0.460	0.560	.0181	.0220
K1	0.460	0.510	.0181	.0201



Unit : mm (inch)

9 Ordering Information

P/N *	Package Type	Pin Count	Package Size
AM5AA085AW	PDIP	8	300mil
AM5AA085AX	SOP	8	150mil
AM5AA085AP	PDIP	14	300mil
AM5AA085AS	SOP	14	150mil
AM5AA171AW	PDIP	14	300mil
AM5AA171AX	SOP	14	150mil
AM5AA171AP	PDIP	18	300mil
AM5AA171AS	SOP	18	150mil

*** Indication of Part Number (P/N):**