DATA SHEET
SPECIFICATION

BMC50x

Turbo 80C51 8-bit
Microcontroller

For

Sound & GPS Device
Home Appliance
General Purpose Application

Revision 0.2

BOOREE
Multimedia Chip & Solution

Boo-Ree
Multimedia Inc.

Scope of this Revision

Revision 0.1 of the User's Manual is intended for system development. Every attempt has been made to ensure a consistent and implemental specification. Implementations should ensure compliance with this revision.

Revision History

Revision	Date	Comments
0.1	2005.08.01	1st released version for customer's development
0.2	2005.11.07	SPEC upgrade and correct errorta in v 0.1

Please send comments via e-mail to support@boo-ree.com
For more information, refer to out web page at http://www.boo-ree.com

1 INTRODUCTION

The BMC50x series combine a powerful 8051-based micro-controller with a hardwired ADPCM decoder, called ***BRAC®***, with which you even could make high-quality voice, sound and simple MIDI Applications. And its maximum 4Mbit embedded e-Flash memory and richer peripherals will reduce the chip count on your system and manufacturing cost. In addition, In-house software development tool kit (***PowerStudio*** : Compiler & Debugger) and hardware emulator (***SimpleICE***) will make your development much faster and easier for your time-to-market release.

1.1 Features

- **Fast 8-bit Turbo 8051 core MCU**
  - Advanced B51core using 2-clocks per instruction
  - Max. 12.5 MIPs performance @ 25MHz
  - Low power 0.25 um e-Flash CMOS technology
  - Dual DPTRs (Data Pointer Registers) for fast block move

- **Hardwired ADPCM Decoder**
  - Embedded Boo-Ree ADPCM Decoder(BRAC®) with DMA
  - Selectable sampling frequency from 8KHz to 48KHz
  - Built-in Low Pass Filter & 3 times up-sampling
  - Volume control with mute feature
  - Automatic DMA access to external Serial Flash (up to 64Mbit)
  - 3-bit / 4-bit data compression

- **Memories**
  - Max 4Mbit embedded NOR Flash Memory for program and data
  - Approx. 180 sec playback duration time (@8KHz sampling and 3-bit data compression) through BRAC®
  - 256 Byte On-chip data SRAM
  - 4KByte On-chip Extended data SRAM
  - Up to 64M bits serial flash expanded

- **JTAG Interface**
  - Debug and In-System Programming through JTAG

- **In-house Development Tools**
  - Boo-Ree C51 compiler and PowerStudio v1.0 (SDK: Software Development Kit), PowerICE(In-Circuit Emulator) and SimpleICE
  - 3rd party tools will be supported later

- **Peripheral Interfaces**
  - 4 channels 10-bit A/D Converter
  - 1 channel 12-bit D/A Converter
  - SPI master only bus controller

- 2 channels UARTs
- SPI master/slave multiplied with SCI
- 3 channels 16-bit Programmable Timer Counter Array with additional PWM and capture input function

- **Other Features**
  - Watchdog timer
  - 24 programmable interrupt sources (10 external interrupt sources)
  - Low power consumption
  - Simple MIDI function provided with S/W library

- **Operating Voltages**
  - 3.3V ± 10% (I/O)
  - 2.5V ± 10% (CPU)

- **I/O and Package type**
  - 46 GPIOs (64TQFP: TBD), 30 GPIOs (48LQFP)
  - 48-pin (7x7 mm) LQFP or 64-pin (10x10 mm) TQFP

Part Number	ROM (e-FLASH)	SRAM	ADC (bit x ch)	DAC (12bit)	ADPCM Decoder	Operating Voltage (V)	GPIO 64TQFP(48LQFP)	Schedule
BMC504	4Mbit	4KB	10 x 4	1 ch	Y	IO: 3.0 ~ 3.6 CPU: 2.25 ~ 2.75	46 (30)	Now
BMC502	2Mbit	4KB	10 x 4	1 ch	Y	IO: 3.0 ~ 3.6 CPU: 2.25 ~ 2.75	46 (30)	TBD

Table 1-1. Device Summary

Notes: TBD = To Be Determined

[Unit: sec]

	Major Sampling Rate						
Compression	**4 KHz**	**6.4 KHz**	**8 KHz**	**16 KHz**	**22 KHz**	**32 KHz**	**44.1 KHz**
3-bit	350	218	180	87	63	44	32
4-bit	262	164	130	66	48	33	24

Table 1-2. Playback duration

1.2 Block Diagram

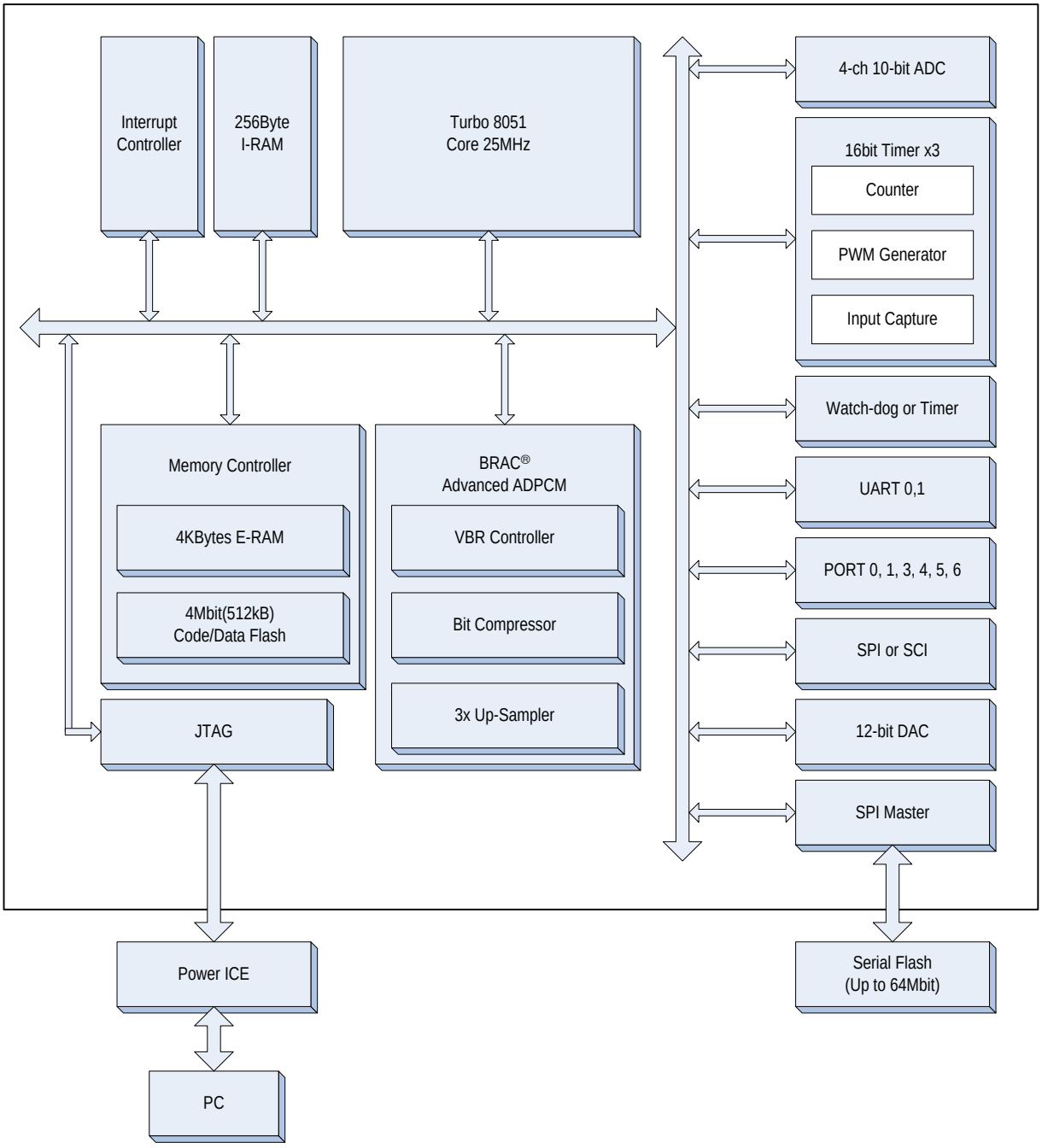
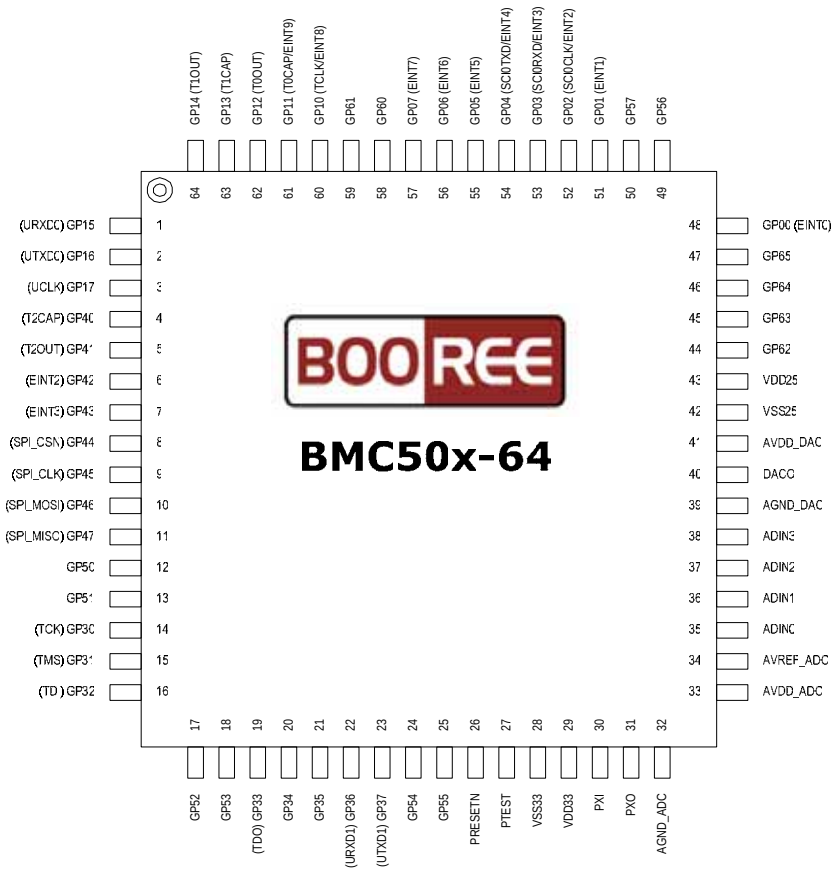
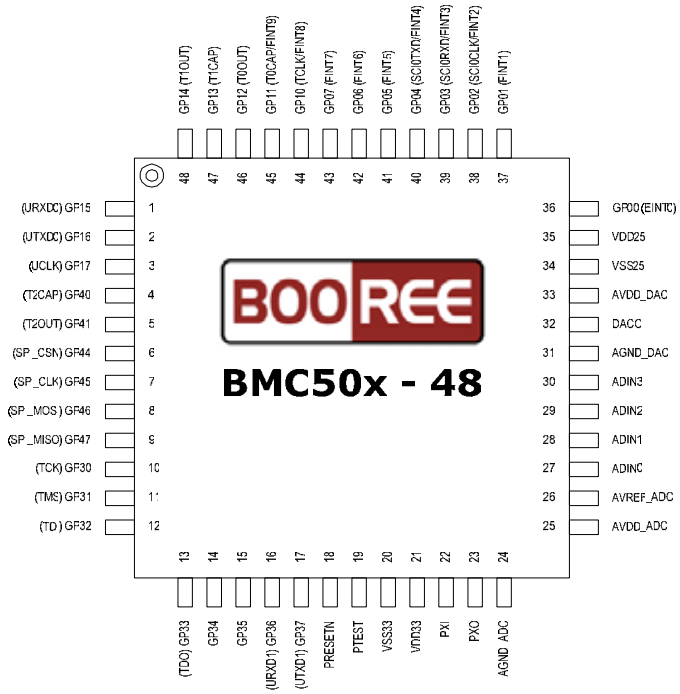


Figure 1-1. Block Diagram

1.3 Pin Assignment





1.4 Pin Descriptions

Pin #		Pin Name	Type	Main Function (After Reset)	Alternate Function
64TQFP	48LQFP				
1	1	GP15/URXD0	I/O	General Purpose I/O 1.5	UART0 Receive Data Input
2	2	GP16/UTXD0	I/O	General Purpose I/O 1.6	UART0 Transmit Data Output
3	3	GP17/UCLK	I/O	General Purpose I/O 1.7	UART0/1 External clock
4	4	GP40/T2CAP	I/O	General Purpose I/O 4.0	Timer input Capture 2
5	5	GP41/T2OUT	I/O	General Purpose I/O 4.1	Timer Output 2
6		GP42	I/O	General Purpose I/O 4.2	
7		GP43	I/O	General Purpose I/O 4.3	
8	6	GP44/SPI_CSN	I/O	General Purpose I/O 4.4	SPI Chip Select
9	7	GP45/SPI_CLK	I/O	General Purpose I/O 4.5	SPI Clock
10	8	GP46/SPI_MOSI	I/O	General Purpose I/O 4.6	SPI Master Output / Slave Input
11	9	GP47/SPI_MISO	I/O	General Purpose I/O 4.7	SPI Master Input / Slave Output
12		GP50	I/O	General Purpose I/O 5.0	
13		GP51	I/O	General Purpose I/O 5.1	
14	10	GP30/TCK	I/O	8051 ICE TCK	General Purpose I/O 3.0
15	11	GP31/TMS	I/O	8051 ICE TMS	General Purpose I/O 3.1
16	12	GP32/TDI	I/O	8051 ICE TDI	General Purpose I/O 3.2
17		GP52	I/O	General Purpose I/O 5.2	
18		GP53	I/O	General Purpose I/O 5.3	
19	13	GP33/TDO	I/O	8051 ICE TDO	General Purpose I/O 3.3
20	14	GP34	I/O	General Purpose I/O 3.4	
21	15	GP35	I/O	General Purpose I/O 3.5	
22	16	GP36/URXD1	I/O	General Purpose I/O 3.6	UART1 Receive Data Input
23	17	GP37/UTXD1	I/O	General Purpose I/O 3.7	UART1 Transmit Data Output
24		GP54	I/O	General Purpose I/O 5.4	
25		GP55	I/O	General Purpose I/O 5.5	
26	18	PRESETN	I	System Reset Pin (active “Low”) with internal Pull-up resistor 100 kΩ	
27	19	PTEST	I	Should be connected Ground	
28	20	VSS33	G	Digital Ground 0V	
29	21	VDD33	P	Digital Power supply 3.3V	
30	22	PXI	I	Clock Input (Max 20MHz)	
31	23	PXO	O	Clock Output	
32	24	AGND_ADC	G	Analog Ground 0V for ADC	
33	25	AVDD_ADC	P	Analog Power Supply 3.3V for ADC	
34	26	AVREF_ADC	P	ADC Reference Top Voltage 3.3V	
35	27	ADIN0	I	Analog Input 0 (Range : 0.0V ~ 3.3V)	
36	28	ADIN1	I	Analog Input 1 (Range : 0.0V ~ 3.3V)	
37	29	ADIN2	I	Analog Input 2 (Range : 0.0V ~ 3.3V)	
38	30	ADIN3	I	Analog Input 3 (Range : 0.0V ~ 3.3V)	
39	31	AGND_DAC	G	Analog Ground 0V for DAC	
40	32	DACO	O	Analog Output of DAC	
41	33	AVDD_DAC	P	Analog Power Supply 3.3V for DAC	
42	34	VSS25	G	Digital Ground 0V	
43	35	VDD25	P	Digital Power supply 2.5V	
44		GP62	I/O	General Purpose I/O 6.2	
45		GP63	I/O	General Purpose I/O 6.3	

46		GP64	I/O	General Purpose I/O 6.4	
47		GP65	I/O	General Purpose I/O 6.5	
48	36	GP00/EINT0	I/O	General Purpose I/O 0.0	External Interrupt 0
49		GP56	I/O	General Purpose I/O 5.6	
50		GP57	I/O	General Purpose I/O 5.7	
51	37	GP01/EINT1	I/O	General Purpose I/O 0.1	External Interrupt 1
52	38	GP02/SCICLK/EINT2	I/O	General Purpose I/O 0.2	SCI Clock / External Interrupt 2
53	39	GP03/SCIRXD/EINT3	I/O	General Purpose I/O 0.3	SCI Receive Data External Interrupt 3
54	40	GP04/SCITXD/EINT4	I/O	General Purpose I/O 0.4	SCI Transmit Data External Interrupt 4
55	41	GP05/SCICSN/EINT5	I/O	General Purpose I/O 0.5	SCI Chip Select External Interrupt 5
56	42	GP06/EINT6	I/O	General Purpose I/O 0.6	External Interrupt 6
57	43	GP07/EINT7	I/O	General Purpose I/O 0.7	External Interrupt 7
58		GP60	I/O	General Purpose I/O 6.0	
59		GP61	I/O	General Purpose I/O 6.1	
60	44	GP10/TCLK/EINT8	I/O	General Purpose I/O 1.0	Timer input Clock 0/1/2 External Interrupt 8
61	45	GP11/T0CAP/EINT9	I/O	General Purpose I/O 1.1	Timer input Capture 0 External Interrupt 9
62	46	GP12/T0OUT	I/O	General Purpose I/O 1.2	Timer Output 0
63	47	GP13/T1CAP	I/O	General Purpose I/O 1.3	Timer input Capture 1
64	48	GP14/T1OUT	I/O	General Purpose I/O 1.4	Timer Output 1

Miscellaneous

PXI	Clock Input (Max. 20MHz) Can be connected to either crystal oscillator or external clock input.
PXO	Clock Output 2㏁ resistor is integrated in this pin. If XI is connected to the external clock input rather than oscillator, the XO should be open.
PRESETN	Chip Reset Signal (active “Low”) This PRESETN pin contains an internal pull up resistor 100㏀. Setting this pin to low level initialize the internal state of the device. Setting the input to high release the reset status. The BMC50x waits for the system clock to be stable, and then set PC to the reset interrupt vector. The elapsing time period for clock stabilization after pin is deactivated is about 500㎲.
PTEST	Factor test input pin. This pin should be connected to Ground.

GPIOs (46pins: 64TQFP, 30pins: 48LQFP)

GP00 ~ GP07 GP10 ~ GP17 GP30 ~ GP37 GP40 ~ GP47 GP50 ~ GP57 GP60 ~ GP65	General Purpose I/O port 0/1/3/4/5/6 Bit programmable input or output mode selected by software. Each of these pins can be used as either any data transfer purpose or specific alternative function defined by user. All GPIO pins except JTAG interface are set to normal data IO input mode after reset is released. If any pins are not to be used, those pins should be connector to Ground, or the related port mode has to be changed to data output mode and left open.

External Interrupt (10pins)

EINT0 ~ EINT9	External Interrupt pins

JTAG System Interface (4pins)

TDO	ICE TDO The default function of this pin is JTAG TDO pin and user program can change this pin as normal GPIO when ICE is not connected.
TDI	ICE TDI The default function of this pin is JTAG TDI pin and user program can change this pin as normal GPIO when ICE is not connected.
TCK	ICE TCK The default function of this pin is JTAG TCK pin and user program can change this pin as normal GPIO when ICE is not connected. In the case of using TCK, internal pull-up resister is connected to this pin automatically.
TMS	ICE TMS The default function of this pin is JTAG TMS pin and user program can change this pin as normal GPIO when ICE is not connected. In the case of using TCK, internal pull-up resister is connected to this pin automatically.

ADC Interface (7pins)

ADIN0 ~ ADIN3	Analog Input 0 ~ 3 (Range: 0.0V ~ 3.3V)
AVREF_ADC	ADC Reference Top Voltage 3.3V
AVDD_ADC	Analog Power Supply 3.3V
AGND_ADC	Analog Ground 0V

DAC Interface (3pins)

DACO	Analog output of DAC
AVDD_DAC	Analog Power Supply 3.3V
AGND_DAC	Analog Ground 0V

Serial Flash Interface (4pins)

SPI_CSN	Chip Select
SPI_CLK	Clock
SPI_MOSI	Data Output
SPI_MISO	Data Input

UART Interface (5pins)

UCLK	External Clock Source for UART 0 and UART 1
URXD0/URXD1	Receive Data Input for UART 0 and UART 1
UTXD0/UTXD1	Transmit Data Output for UART 0 and UART 1

SCI/SPI Interface (4pins)

SCI0CLK	External Clock Source for Serial Communication Interface
SCI0RXD	Receive Data Input for Serial Communication Interface
SCI0TXD	Transmit Data Output for Serial Communication Interface
SCI0CSN	Chip Select for SPI operation

Timer Interface (7pins)

TCLK	External Clock Source for Timer 0, Timer 1 and Timer 2

T0CAP/T0OUT	Timer 0 Capture input / Timer 0 16-bit PWM mode output or counter match toggle output
T1CAP/T1OUT	Timer 1 Capture input / Timer 1 16-bit PWM mode output or counter match toggle output
T2CAP/T2OUT	Timer 2 Capture input / Timer 2 16-bit PWM mode output or counter match toggle output

2 Electric Characteristics

2.1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{OPR}	Operating ambient temperature	-40	-	85	℃
P_D	Power dissipation (@ 2.5V)				㎽
V_I	Input pin voltage	-0.3	-	V_{DD} +0.3	V
V_O	Output pin voltage	-0.3	-	V_{DD} +0.3	V

2.2 Operating Conditions

Ta = -40 ℃ to 80 ℃

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DSP}	Digital Supply Voltage	2.3	2.5	2.7	V
V_{IOSP}	IO Supply Voltage	3.0	3.3	3.6	V
V_{ASP}	Analog Supply Voltage	3.0	3.3	3.6	V
F_{XTAL}	Crystal Oscillator	1.0	-	25	㎒
C_{XTAL}	External capacitors		20		pF
R_{XTAL}	Internal Feedback resistor		700		kΩ

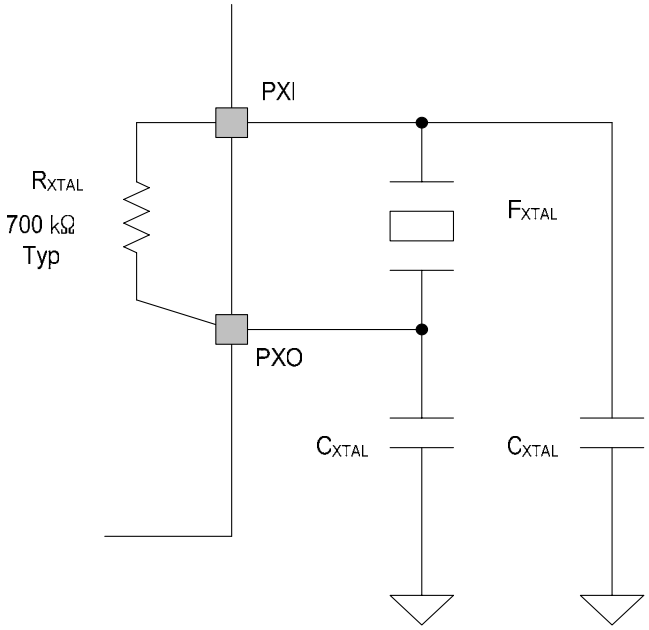


Figure 6-1. Crystal Oscillator

2.3 DC Characteristic

V_{IOSP} = 3.3 ± 0.3 V, Ta = -40 ℃ to 80 ℃

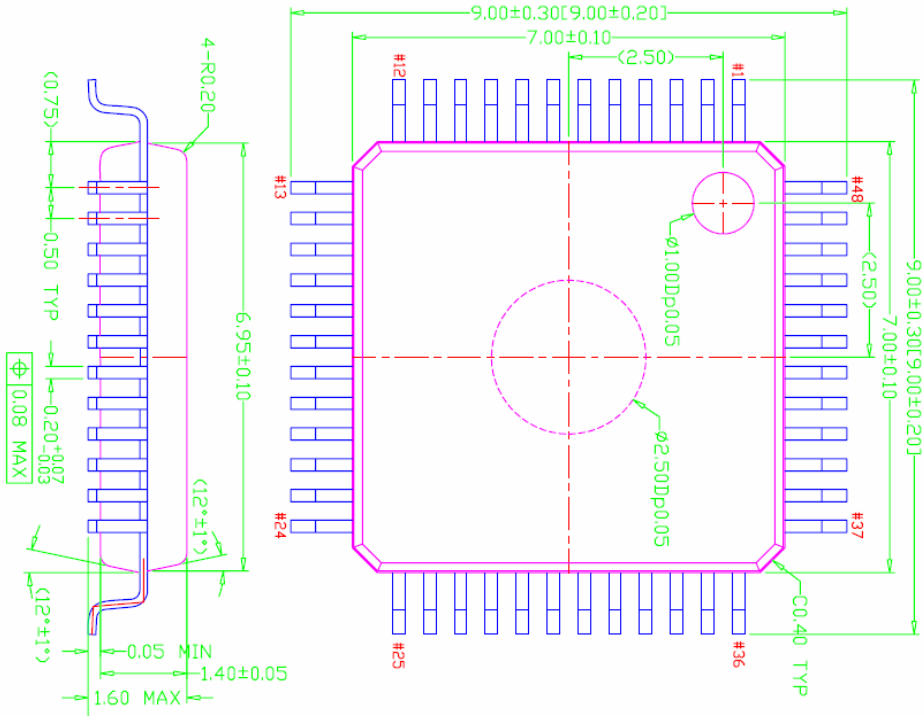
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{OH}	High level output voltage	IOH = -4mA	2.4			V
V_{OL}	Low level output voltage	IOL = 4mA			0.4	V
V_{IH}	High level input voltage	CMOS Schmitt trigger interface	0.8 V_{DD}		VDD	V
V_{IL}	Low level input voltage	CMOS Schmitt trigger interface			0.2 V_{DD}	V
I_I	Input current	V_{IN} = V_{IOSP}	-10		10	μA
	Input current with 40kΩ pull down		40		160	
	Input current with 40kΩ pull up		-160		40	
IDD1	Power supply current	V_{DD}=3.3V F_{XTAL}=20MHz Fsys=10MHz		10		mA
IDD2	Supply current during IDLE mode				100	μA
IDD3	Supply current during STOP mode			10	30	μA

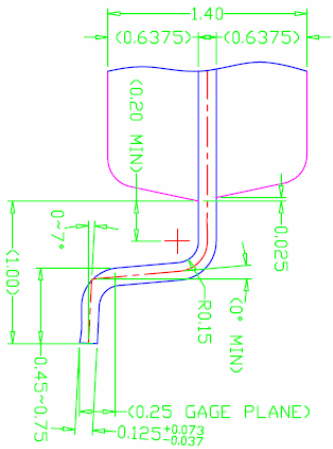
Notes:

PTEST	CMOS Schmitt trigger Input pin with 40kΩ pull down
PRESET	CMOS Schmitt trigger Input pin with 40kΩ pull up
P30, P31	pin with 40kΩ pull up when JTAG mode is enabled
P00 ~ P07	CMOS Schmitt trigger interface
P10 ~ P17	CMOS Schmitt trigger interface
P30 ~ P31	CMOS Schmitt trigger interface with 40kΩ pull up when JTAG mode is enabled
P32 ~ P37	CMOS Schmitt trigger interface
P40 ~ P47	CMOS Schmitt trigger interface
P50 ~ P57	CMOS Schmitt trigger interface
P60 ~ P65	CMOS Schmitt trigger interface

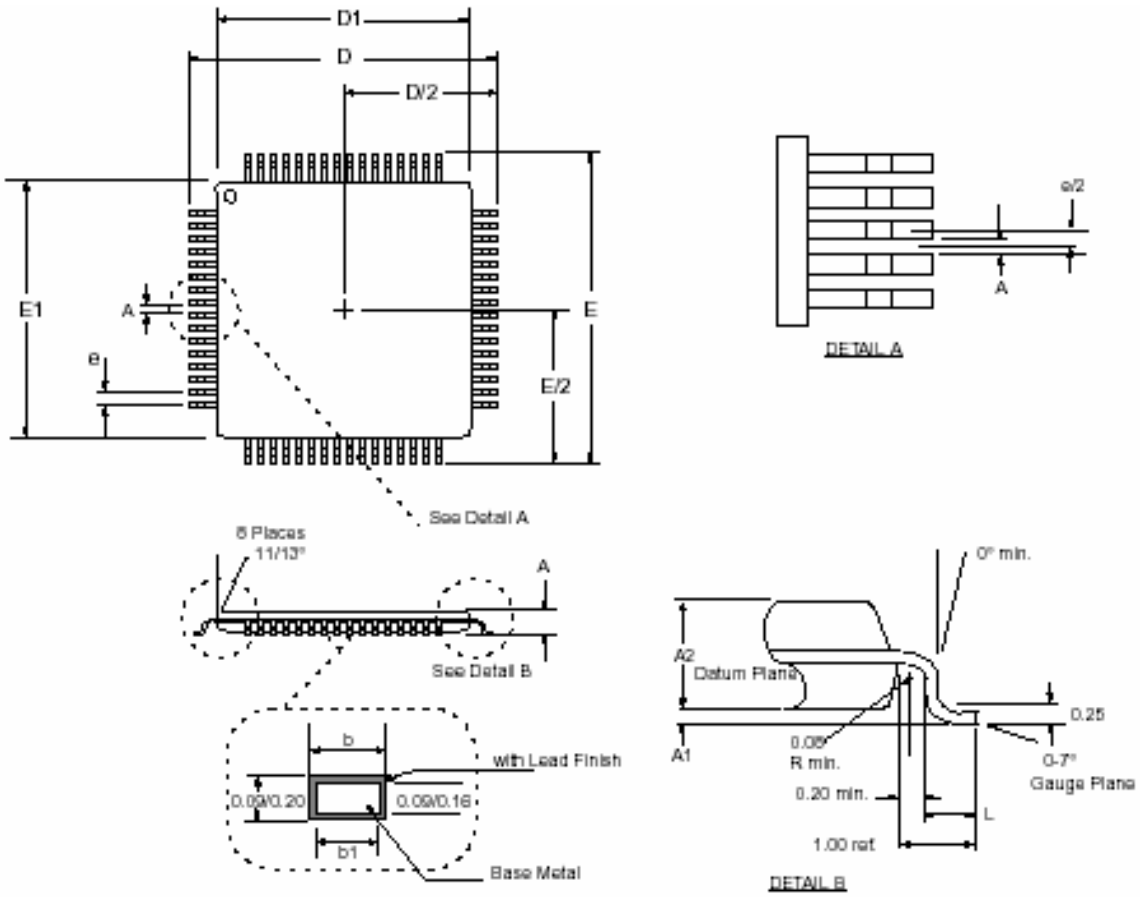
3 PACKAGE DIMENSION

3.1 48LQFP





3.2 64TQFP


D1
D
D/2
E1
A
e
E
E/2
See Detail A
6 Places
11/13°
A
See Detail B
b
with Lead Finish
0.09/0.20
0.09/0.16
b1
Base Metal
e/2
A
DETAIL A
0° min.
A2
Datum Plane
A1
0.08
R min.
0.20 min.
1.00 ref
0.25
0-7°
Gauge Plane
L
DETAIL B